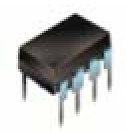

Subject: Electronics Cooling	Author: Mark Biegert
Title: Review of Apex App Note AN51U	**Manager:**
Keywords: thermal, resistance, example, power	**Checked By:** Self

Units

Abstract

This paper documents my quick look at Apex App Note AN51U, which provides an example of how to estimate the thermal resistance of a HSOP packaged part. I am just using this app note as a learning vehicle and do not have a specific application in mind.

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Analysis

Thermal Conduction Constants

$$\lambda_{Si} := 148 \frac{W}{m \cdot K}$$

Wikipedia lists 149 W/m K. This is what Apex used.

http://en.wikipedia.org/wiki/Silicon

$$\lambda_{Cu} := 384 \frac{W}{m \cdot K}$$

Wikipedia lists 401 W/m K for pure copper. I see 384 W/m K used quite a bit for the Cu alloys in PCBs.

http://en.wikipedia.org/wiki/Copper

$$\lambda_{FR4} := 0.26 \frac{W}{m \cdot K}$$

Wikipedia cites two sources with different values, 0.29 W/m K and 0.343 W/m K.

http://en.wikipedia.org/wiki/FR-4

$$\lambda_{Slug} := 220 \frac{W}{m \cdot K}$$

The heat slug is usually constructed of Al, Ni or an alloy of Cu and Mo. This number is reasonable for an Al slug.

http://en.wikipedia.org/wiki/Aluminum

Overall Thermal Model

The paper uses the resistive thermal model shown below.

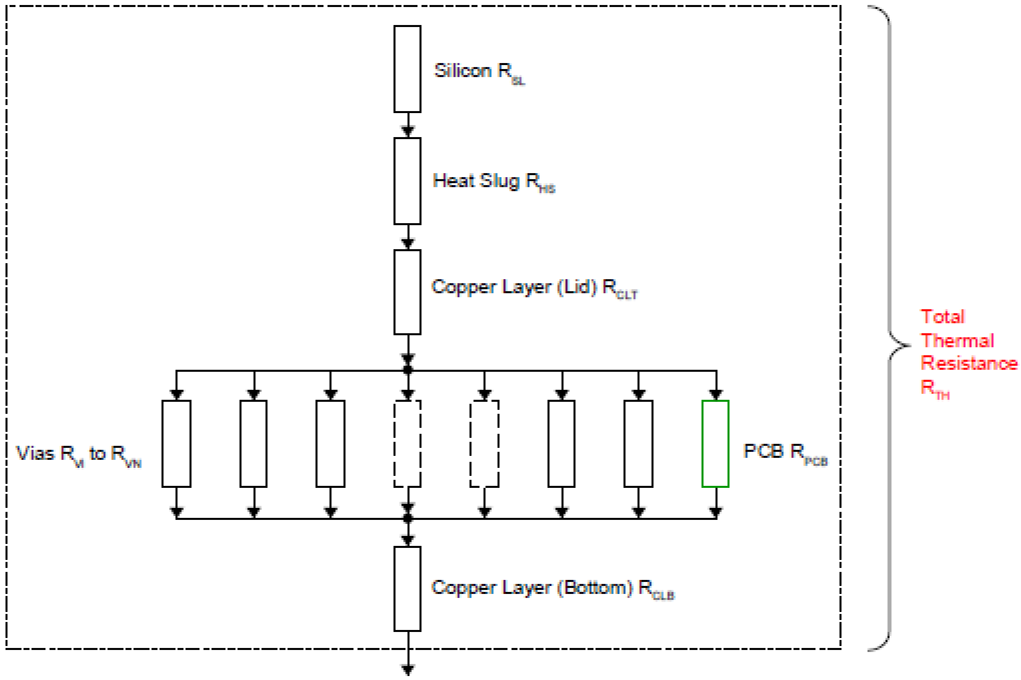
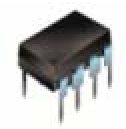


Figure 2: Equivalent thermal circuit for the power IC – circuit board configuration



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Thickness of a Cu Layer Based on Its "Weight"

PCB copper thickness is usually expressed in terms of the weight (mass) of a 1 square foot sheet. Common values are 0.5 oz, 1 oz, and 2 oz. Let's convert this odd measure into a thickness.

$\rho_{Cu} := 8.96 \dfrac{\mathbf{gm}}{\mathbf{cm}^3}$ *http://en.wikipedia.org/wiki/Copper*

$A_{Cu} := 1\mathbf{ft}^2$ *Reference area for "old school" definition of thickness.*

$m_{Cu} = A_{Cu} \cdot \tau_{Cu} \cdot \rho_{Cu}$ *Let τ_{Cu} be the thickness of the Cu plate.*

$\tau_{Cu}(m_{Cu}) := \dfrac{m_{Cu}}{A_{Cu} \cdot \rho_{Cu}}$ *Formula for the thickness of Cu sheet as a function of mass*

Example Calculations

$$\tau_{Cu}\begin{pmatrix} 0.5\mathbf{oz} \\ 1\mathbf{oz} \\ 2\mathbf{oz} \end{pmatrix} = \begin{pmatrix} 0.67 \\ 1.341 \\ 2.682 \end{pmatrix} \cdot \mathbf{mil}$$ *I see this thickness value quoted frequently.*

Thermal Resistance of Heat Slug Within the Part

$l_{Slug} := 1\mathbf{mm} = 39.37 \cdot \mathbf{mil}$ *Length listed by Apex. I do not have an easy way to verify it.*

$A_{Slug} := 100 \cdot 10^{-6} \cdot \mathbf{m}^2$ *This is the value listed in the Apex example.*

$R_{HS} := \dfrac{1}{\lambda_{Slug}} \cdot \dfrac{l_{Slug}}{A_{Slug}} = 0.045 \cdot \dfrac{\mathbf{K}}{\mathbf{W}}$ ✓ *This example checks with Apex work.* E3 D1

My Take on These Numbers

Based on the package drawing, here is what I would have used.

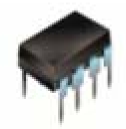
$\mathbf{w} := 6.85\mathbf{mm}$ *HSOP 44 pin package heat slug width*

$\mathbf{l} := 12.15\mathbf{mm}$ *HSOP 44 pon package heat slug length*

⇨ $A_{SlugMe} := \mathbf{w} \cdot \mathbf{l} = 83.228 \cdot 10^{-6} \mathbf{m}^2$

$\therefore \dfrac{A_{Slug}}{A_{SlugMe}} = 1.202$ *These values are relatively close.*

Thermal Resistance of a Via in the PCB



A via is modeled as a cylinder of Cu the penetrates the circuit board. It is specified by its outside diameter. The plating of the via with Cu reduces the diameter of the hole.

$$A_V(\tau, d_0) := \left| \begin{array}{l} d \leftarrow -2\tau + d_0 \\ \pi \cdot \left(\dfrac{d_0^{\,2} - d^2}{4} \right) \end{array} \right.$$

See Anatomy of a Via for details

Link to Online Calculator Example

$l_{Via} := 1.5\,\mathbf{mm} = 59.1 \cdot \mathbf{mil}$ ***Apex value***

$A_{Via} := 6.28 \cdot 10^{-8} \cdot \mathbf{m}^2 = 97 \cdot \mathbf{mil}^2$ ***Apex Value***

$$R_{Via} := \frac{1}{\lambda_{Cu}} \cdot \frac{l_{Via}}{A_{Via}} = 62.201 \cdot \frac{\mathbf{K}}{\mathbf{W}}$$

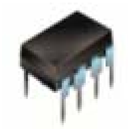
No Apex value listed.

My Take on These Numbers

$l_{Via} = 59.055 \cdot \mathbf{mil}$ ***We commonly see vias specified at 60 mils.***

I would normally see our 20 mil vias have this area of Cu.

$A_V(\tau_{Cu}(1\mathbf{oz}), 20\mathbf{mil}) = 79 \cdot \mathbf{mil}^2$ ***This is close to the Apex value.***



Thermal Resistance of the Silicon Die

We normally do not see the silicon's thermal resistnance discussed because it is lumped in with other parameters. It is interesting to think about the impact it has.

$l_{SL} := 0.38\,\mathbf{mm} = 15 \cdot \mathbf{mil}$ *Standard thickness of a chip from a 3 inch wafer.*

http://en.wikipedia.org/wiki/Silicon_wafer#Standard_wafer_sizes

$A_{SL} := 15.8 \cdot 10^{-8} \cdot \mathbf{m}^2 = 244.9 \cdot \mathbf{mil}^2$ *Apex Value. This does not seem correct. It is way too small. I would expect a part about 100 mil square.*

$$R_{SL} := \frac{1}{\lambda_{Si}} \cdot \frac{l_{SL}}{A_{SL}} = 16.25 \cdot \frac{\mathbf{K}}{\mathbf{W}}$$

Not the value Apex got. Normally, an analog IC die like this will be rectangular with dimensions around 100 mil square.

$A_{SL} := (100\,\mathbf{mil})^2 = 6.452 \times 10^{-6}\,\mathbf{m}^2$ *Let's try my nominal dimensions and see how they work.*

$$R_{SL} := \frac{1}{\lambda_{Si}} \cdot \frac{l_{SL}}{A_{SL}} = 0.398 \cdot \frac{\mathbf{K}}{\mathbf{W}}$$ ✓

This is very near the Apex value of 0.405 K/W. I will use this value in my calculations below.

Thermal Resistance of the Cu Top Layer of the PCB

Assume a Cu thermal pad is put on the top layer of the PCB.

$l_{CLT} := 0.035\,\mathbf{mm} = 1.378 \cdot \mathbf{mil}$ *Standard 1 ozf Cu.*

$A_{CLT} := 100 \cdot 10^{-6} \cdot \mathbf{m}^2$ *Thermal pad will be the same size as the heat slug.*

$$R_{CLT} := \frac{1}{\lambda_{Cu}} \cdot \frac{l_{CLT}}{A_{CLT}} = 9.115 \times 10^{-4} \cdot \frac{\mathbf{K}}{\mathbf{W}}$$

✓ *Agrees with Apex.*

Thermal Resistance of the Cu Bottom Layer of the PCB

Assume this is a plane along the entire bottom of the PCB.

$l_{CLB} := 0.035\,\mathbf{mm} = 1.378 \cdot \mathbf{mil}$ *Standard 1 ozf (1 ounce force) of Cu per square foot.*

$A_{CLB} := 2160 \cdot 10^{-6} \cdot \mathbf{m}^2 = 3.348 \cdot \mathbf{in}^2$ *Thermal pad will be the same size as the heat slug.*

If square, the PCB would have a side length of $\sqrt{A_{CLB}} = 1.83 \cdot \mathbf{in}$

$$R_{CLB} := \frac{1}{\lambda_{Cu}} \cdot \frac{l_{CLB}}{A_{CLB}} = 4.22 \times 10^{-5} \cdot \frac{\mathbf{K}}{\mathbf{W}}$$

Disagrees with Apex, but this number is so small it doesn't matter.

Thermal Resistance of the PCB

Assume we are working with FR4 with the same area as the heat slug.

$l_{PCB} := 1.5\,\mathrm{mm} = 59.055 \cdot \mathrm{mil}$ ***Apex assumption. Common board thickness.***

$A_{PCB} := 100 \cdot 10^{-6} \cdot \mathrm{m}^2 = 1.55 \times 10^5 \cdot \mathrm{mil}^2$ ***Thermal pad will be the same size as the heat slug.***

$$R_{PCB} := \frac{1}{\lambda_{FR4}} \cdot \frac{l_{PCB}}{A_{PCB}} = 57.692 \cdot \frac{\mathrm{K}}{\mathrm{W}}$$

No Apex number given. This result is consistent with the data they present.

This thermal resistance dominates all the other thermal resistances on the PCB. This is why we add a large number of vias to provide a thermal bridge.

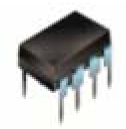
Thermal Resistance of the PCB with 24 Vias

They do not give you all the information you need to generate this number, so we need to make some reasonable assumption about the number of vias. The vias will be modeled as parallel thermal resistances.

$N_{Via} := 24$ ***I picked this number so that I get the PCB resistance that Apex listed. It is reasonable number and probably what they used.***

$$R_{PCB} := \frac{1}{\frac{1}{R_{PCB}} + \frac{N_{Via}}{R_{Via}}} = 2.4803 \cdot \frac{\mathrm{K}}{\mathrm{W}} \checkmark$$

Agrees with Apex.



Overall Thermal Resistance Number

This is the first time I have seen someone model the silicon.

My overall number agrees with the final result from Apex.

$$R_{Total} := R_{SL} + R_{HS} + R_{PCB} + R_{CLT} + R_{CLB} = 2.925 \cdot \frac{K}{W}$$

Silicon die
Heat Slug
Fiberglass and vias
Copper top layer
Copper bottom layer

$i := 0 .. 4$

✓ *Overall Result Agrees with Apex.*

$$R_{tmp} := \begin{pmatrix} R_{SL} \\ R_{HS} \\ R_{PCB} \\ R_{CLT} \\ R_{CLB} \end{pmatrix} = \begin{pmatrix} 0.397974 \\ 0.045455 \\ 2.480303 \\ 0.000911 \\ 0.000042 \end{pmatrix} \cdot \frac{K}{W}$$

$$\frac{R_{tmp}}{\left(\sum_i R_{tmp_i}\right)} = \begin{pmatrix} 13.61 \\ 1.55 \\ 84.81 \\ 0.03 \\ 0 \end{pmatrix} \cdot \%$$

Reference Article

Adobe Acrobat Document

Zip File of Apex Datasheet AN51U. I have noticed that PDFs sometimes get corrupted.