Design Metrics in VLSI Design

[Adapted from Rabaey’s Digital Integrated Circuits, ©2002, J. Rabaey et al.]

Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
  - design time and effort, mask generation
  - one-time cost factor
- Recurrent costs
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area

NRE Cost is Increasing

From http://www.amd.com

Die Cost

Single die

Wafer

Going up to 12” (30cm)
Cost per Transistor

Yield

Yield = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%

Die cost = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}

Dies per wafer = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}

Defects

Yield = 25\%

\text{die yield} = \left(1 - \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{\text{defects per unit area} \times \text{die area}}^\alpha

\alpha \text{ is approximately } 3

\text{die cost} = f(\text{die area})^\alpha

Example

- You want to start a company to build a wireless communications chip. How much venture capital must you raise?
  - Because you are smarter than everyone else, you can get away with a small team in just two years:
    - Seven digital designers
    - Three analog designers
    - Five support personnel

Solution

- Digital designers:
  - $70k salary
  - $30k overhead
  - $10k computer
  - $10k CAD tools
  - Total: $120k * 7 = $840k
- Analog designers:
  - $100k salary
  - $30k overhead
  - $10k computer
  - $100k CAD tools
  - Total: $240k * 3 = $720k

- Support staff
  - $45k salary
  - $20k overhead
  - $5k computer
  - Total: $70k * 5 = $350k

- Fabrication
  - Back-end tools: $1M
  - Masks: $1M
  - Total: $2M / year

- Summary
  - 2 years @ $3.91M / year
  - $8M design & prototype
Reliability—Noise in Digital Integrated Circuits

(a) Inductive coupling (b) Capacitive coupling (c) Power and ground noise

DC Operation
Voltage Transfer Characteristic

VOH = f(VOL)
VOL = f(VOH)
VM = f(VM)

Mapping between analog and digital signals

Gate Output → Gate Input

VOH
VOL

"0"
VOL

"1"
VOH

V(y) = V(x)

Switching Threshold

Undefined Region

VOH = f(VOL)
VOL = f(VOH)
VM = f(VM)

Noise Budget

- Allocates gross noise margin to expected sources of noise
- Differentiate between fixed and proportional noise sources
- Sources: supply noise, cross talk, interference, offset
- Shielding: metal lines and guard rings used to lower signal interference

Definition of Noise Margins

Noise margin high

Noise margin low

Key Reliability Properties

- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- Noise immunity is the more important metric – the capability to suppress noise sources
- Key metrics: Noise transfer functions, Output impedance of the driver and input impedance of the receiver;
Regenerative Property

- Regenerative
- Non-Regenerative

Fan-in and Fan-out

- **Fan-out:**
  - Number of load gates, \( N \), that are connected to the output of the driving gate
  - tends to lower the logic levels
  - deteriorates dynamic performance
  - gate must have low output resistance to drive load
  - library cells have maximum fan-out specification
- **Fan-in:**
  - Number of inputs, \( M \), to the gate
  - large fan-in gates are more complex
  - results in inferior static and dynamic performance

The Ideal Gate

Characteristics

- \( R_i = \infty \)
- \( R_o = 0 \)
- Fanout \( = \infty \)
- \( \text{NMH} = \text{NML} = \text{VDD}/2 \)

An Old-time Inverter
**Delay Definitions**

- $V_{out}$
- $V_{in}$
- $t_{pLH}$
- $t_{pHL}$
- $t_{r}$
- $t_{f}$

**Ring Oscillator**

$$T = 2 \times t_{p} \times N$$

**A First-Order RC Network**

$V_{out}(t) = (1 - e^{-t/\tau}) \cdot V$

$$t_{p} = \ln(2) \cdot \tau = 0.69 \cdot RC$$

Important model – matches delay of inverter

**Power Dissipation**

- Instantaneous power:
  $$p(t) = v(t) \cdot i(t) = V_{supply} \cdot i(t)$$
- Peak power:
  $$P_{peak} = V_{supply} \cdot i_{peak}$$
- Average power:
  $$P_{ave} = \frac{1}{T} \int_{0}^{T} p(t) \cdot dt = \frac{V_{supply}}{T} \int_{0}^{T} i_{supply} \cdot (t) \cdot dt$$

**Energy and Energy-Delay**

- Power-Delay Product (PDP) = $E = \text{Energy per operation} = P_{ave} \times t_{p}$
- Energy-Delay Product (EDP) = quality metric of gate = $E \times t_{p}$

**A First-Order RC Network**

$$E_{0 \rightarrow x} = \frac{T}{0} \int_{0}^{Vdd} P_{out}(t) dVout = \frac{T}{0} \int_{0}^{Vdd} i_{supply}(t) dVout = V_{dd} \cdot C_{L} \cdot \left( V_{out} - V_{out} \right)$$

$$E_{cap} = \frac{T}{0} \int_{0}^{Vdd} P_{cap}(t) dVcap = \frac{T}{0} \int_{0}^{Vdd} i_{cap} dVcap = V_{dd} \cdot \frac{1}{2} \cdot C_{L} \cdot \left( V_{dd} - V_{out} \right)^{2}$$
Digital integrated circuits have come a long way and still have some potential left for the coming decades.

Some interesting challenges ahead:
- Getting a clear perspective on the challenges and potential solutions
- Understanding the design metrics that govern digital design is crucial
- Optimize the design metrics - cost, reliability, speed, power and energy dissipation