References

Link Power Electronics reference article

Link Good Synquor example

Constants

$P_O := 200\mathbf{W}$ Load power

$V_{I\_max} := 36\mathbf{V}$ Maximum input voltage

$V_{I\_min} := 18\mathbf{V}$ Minimum input voltage

$\eta := 83\%$ Load power converter conversion efficiency

Analysis

Switching Supply Input Resistance is Negative (at least for low frequencies)

$$P_I = \frac{P_O}{\eta} = V_I \cdot I_I$$ Definition of power and efficiency

$$I_I := \frac{P_O}{\eta \cdot V_{I\_max}} = 6.69\mathbf{A}$$ Substitute example values, this would be the input current.

Definition of differential input resistance

$$r_d(P, I_I) := \frac{d}{dI_I}\frac{P}{I_I} \rightarrow -\frac{P}{{I_I}^2} \qquad r_d(V_I, I_I) := r_d(V_I \cdot I_I, I_I) \rightarrow -\frac{V_I}{I_I}$$

$$r_d(V_{I\_max}, I_I) = -5.38\Omega$$ Example differential resistance SynQuor example of actual input resistance

Switching Supply is Equivalent to a DC Transformer

Ignoring the inefficiency

$$V_I \cdot I_I = V_O \cdot I_O$$

$$\frac{V_I}{V_O} = \frac{I_O}{I_I} = n$$ n being equivalent to the turns ratio. $n = D$ where n is the duty cycle of the switcher

Let $R_L = V_O / I_O$

$$V_I = V_O \cdot n = \frac{V_O}{I_O} \cdot n \cdot I_O = n \cdot R_L \cdot I_O \Rightarrow I_I = \frac{I_O}{n}$$

$$r_d(n, R_L) := r_d\left(n \cdot R_L \cdot I_O, \frac{I_O}{n}\right) \rightarrow -R_L \cdot n^2$$ Very similar to the impedance transformation formula for a transformer.

Analysis of Typical Example

Example of a Typical Zero-Current Switcher (ZCS).

Fig. 1. A commercial dc-dc converter that employs zero current switching.

Remember that this note was by a Vicor PLM person.

Rule of thumb is that the source impedance should be less than 10 % that of the supply input impedance.

$$Z_{S\_max} := \left| \frac{V_{LL}}{P_{LL}} \cdot V_{LL} \cdot \frac{1}{10} \right|$$

V_{LL} is the low line input voltage
P_{LL} is the low line input power of the module

Uncompensated Case

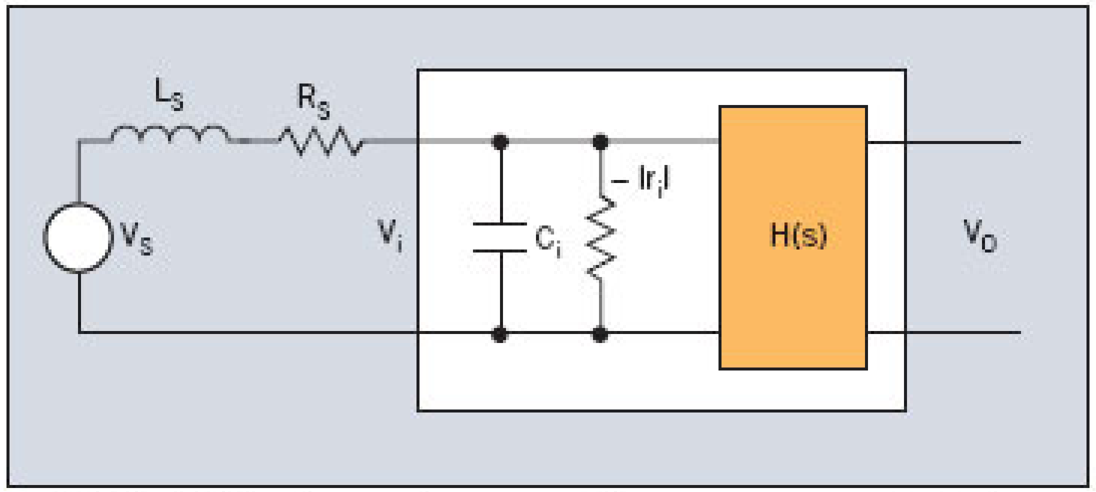

Fig. 2. A typical dc-dc converter connects to a power source having its own internal impedance, which is not zero.

$$eq1 := H(s)\cdot V_S\cdot\frac{\dfrac{\frac{1}{s\cdot C_i}\cdot -r_i}{\frac{1}{s\cdot C_i}+-r_i}}{R_S+s\cdot L_S+\dfrac{\frac{1}{s\cdot C_i}\cdot -r_i}{\frac{1}{s\cdot C_i}+-r_i}}\ \text{simplify}\ \rightarrow$$

The denominator is referred to as the characteristic polynomial and determines the stability of the system.

$$eq2 := \frac{\text{denom}(eq1)}{r_i}\ \text{simplify}\ \rightarrow$$

This is the characteristic polynomical of this equation.

$$eq3 := eq2\ \text{coeffs}, s\ \rightarrow$$

To ensure negative roots, all coefficients must be positive (Decartes' rule of sign)

$eq3_0 > 0 \rightarrow 1 - \frac{R_S}{r_i} > 0$ (1) $r_i > R_S$ ✓ **Same result as in the article**

L_S **Same result as in the article**

Compensated Power Supply Input

$eq3_1 > 0 \rightarrow C_i \cdot R_S - \frac{}{r_i} > 0$ (2) $R_S > \frac{L_S}{C_i \cdot r_i}$ ✓

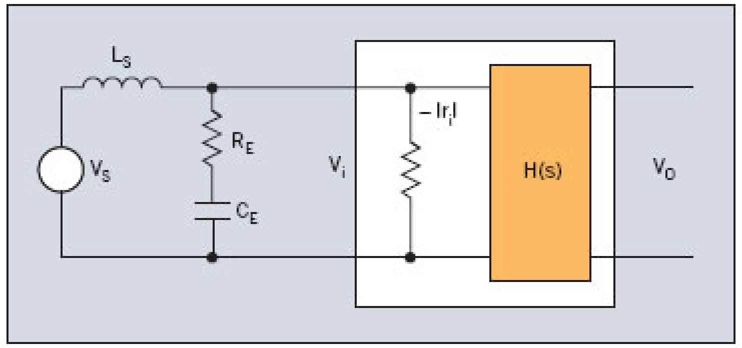

Fig. 3. A common practice is to put a large capacitor in parallel with the input stage of a dc-dc converter.

Compared to Figure 2, the resistance, R_S, has been removed to simplify the analysis.

$$eq4 := H(s) \cdot \frac{\dfrac{1}{\dfrac{1}{\dfrac{1}{s \cdot C_E} + R_E} - \dfrac{1}{r_i}}}{s \cdot L_S + \dfrac{1}{\dfrac{1}{\dfrac{1}{s \cdot C_E} + R_E} - \dfrac{1}{r_i}}} \text{ simplify } \rightarrow$$

$$r_i > R_E > \frac{L_S}{C_S \cdot r_i}$$

$eq5 := \text{denom}(eq4) \rightarrow$

$eq6 := eq5 \text{ coeffs}, s \rightarrow$

To ensure negative roots, all coefficients must be positive

$eq7 := eq6_1 > 0 \rightarrow$ (3) $r_i > \frac{L_S}{C_E \cdot R_E}$ ✓ Same result as in the Power Electronics and Synquor articles.

$eq8 := eq6_2 > 0 \rightarrow$ (4) $r_i > R_E$ ✓ Same result as in the Power Electronics and Synquor articles.

Eq. 4 states that R_E should be smaller than r_i. However, from Eq. 3, it is clear that if R_E is made too small, oscillation will result. This means that adding low-ESR capacitance may not resolve a stability problem – more loss is needed.

From Eq. 3, it is also possible to see that a bigger input inductance requires a larger input capacitance to compensate its effects. Also, lower input differential resistance, r_i, means a larger input capacitance is needed to ensure stable operation. Once the value of the input inductor, L_S, and input incremental resistance, r_i, are known, it is possible to replace the numbers in Eq. 3 and 4 to find the optimal combination for C_E with the proper ESR.

Appendix

Example of an Actual Power Supply Input Impedance

Figure 2 shows $|Z_I|$ versus frequency for SynQor's $48V_{IN}$, $3.3V_{OUT}$, 30A dc/dc converter. As can be seen, at low frequencies $|Z_I|$ is resistive (actually, we need to look at the phase of Z_I, which is -180° at low frequencies, to see that it is negative). Around 1 kHz the magnitude starts to roll off with a slope of -20dB per decade. We can model this as a capacitor C in parallel with R_N. Similarly, a more complex circuit can model the resonant dynamics that show up around 20 kHz in the plot of $|R_N|$. For this discussion, however, we will just use the simple R_NC model.

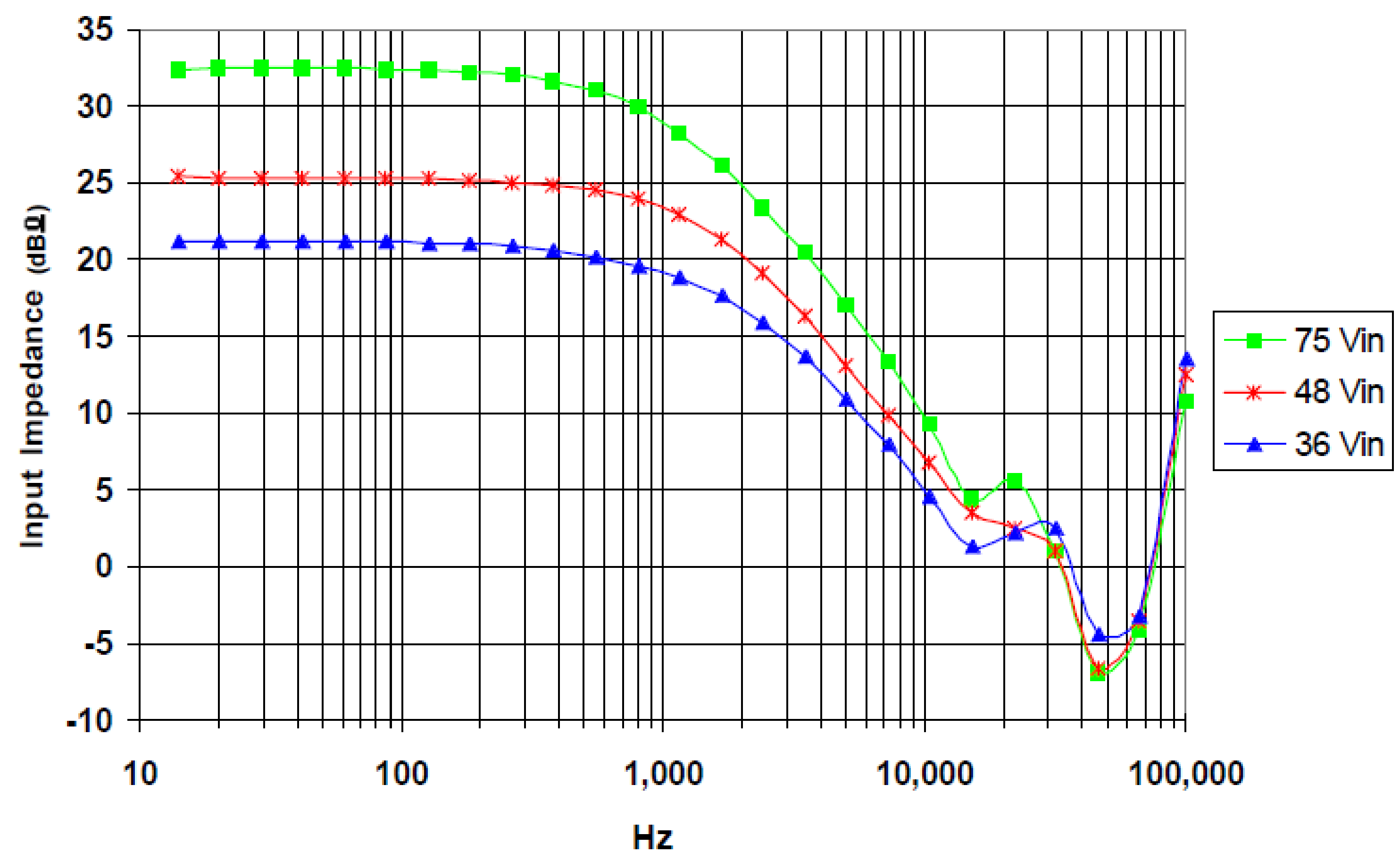

Figure 2: *Input impedance ($Z_I = V_{IN}/I_{IN}$) for minimum, nominal, and maximum input voltage at full rate power for $3.3V_{OUT}$, 30A half-brick dc/dc converter.*