

# ANATOMY OF A PLATED THROUGH HOLE

LEE RITCHEY

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## INTRODUCTION

This document examines the way a plated through hole is formed in a PCB. The discussion holds whether the hole is used by a signal to change layers (usually called a via) or to connect a component pin to a plane or signal line. It also holds when the hole is not plated, such as for mounting hardware. It is important to understand this in order to correctly calculate the sizes of pads and keep out areas needed to insure the PCB is both manufacturable and meets its electrical requirements.

A clear understanding of this subject is necessary in order to satisfy the dual needs of assembly and PCB fabrication. The PCB assembler works with finished hole size. The fabrication process is based on the drilled hole size. Along with all of this, it is necessary to size holes in such a way that the power planes of the PCB are not degraded by placing holes so close together that they cause slots to be created in the planes by overlapping clearance holes. It is not possible to specify generously large hole sizes and insulation spacing to make manufacturing or fabrication easy without risking degradation of the environment needed by the high speed signals travelling across those planes through the PCB.

Figure 1 is a picture showing the important structures involved in making a plated through hole.

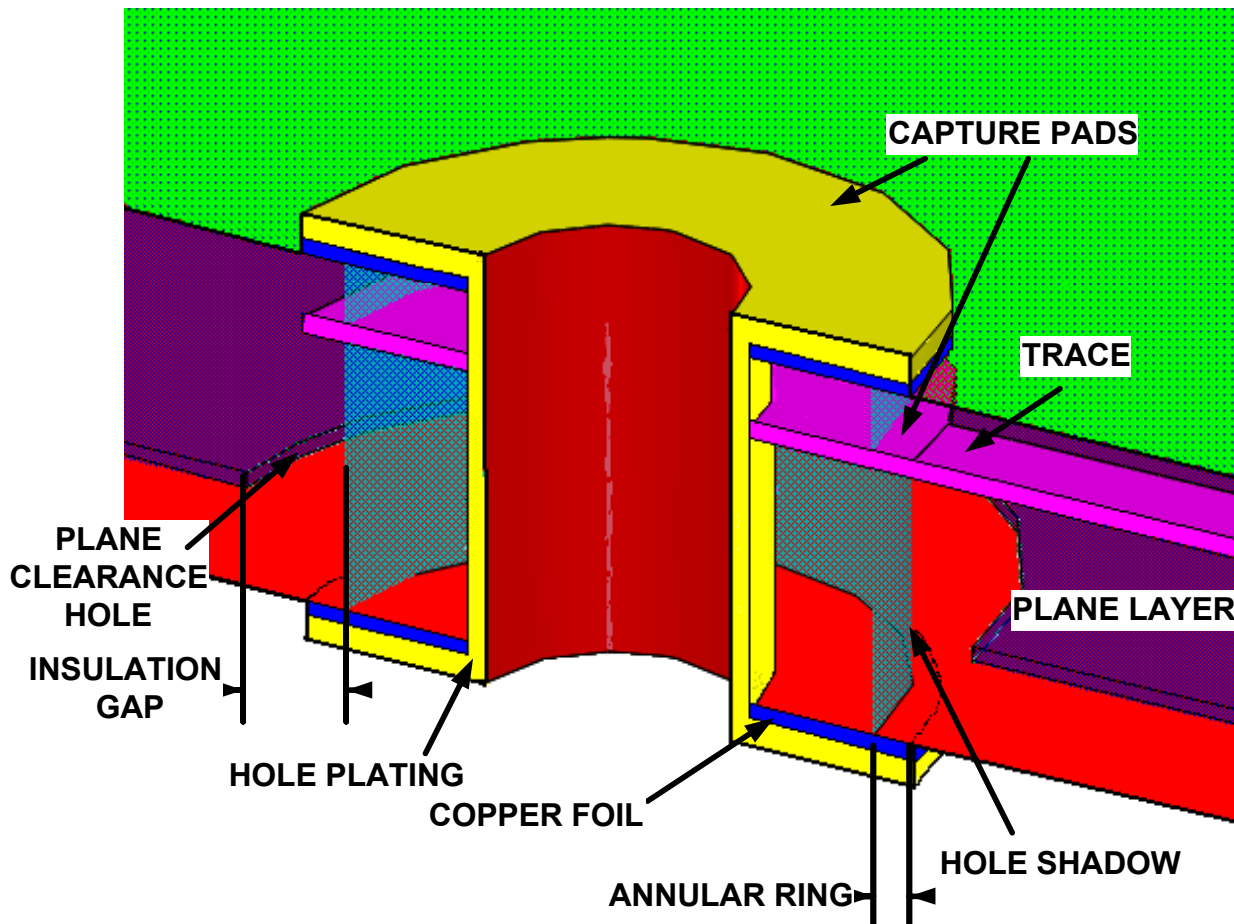


FIGURE 1, CROSS SECTION OF A PLATED THROUGH HOLE OR VIA.

## DEFINITIONS

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Author: Lee W. Ritchey

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The following terminology is used to describe the various components involved in creating a plated through hole. They apply whether the hole is used as a routing via, a component hole or a power connection.

**Finished hole size-** the diameter of the plated through hole after all plating steps are completed.

**Drilled hole size-** the diameter of the hole after drilling.

**Capture pad-** the pads placed on outer layers to “capture” the plated through hole or on inner layers to connect traces to the plated through hole. Capture pads are used on inner layers only when a connection is being made to a trace. Putting capture pads on inner layers where no connections are being made are called nonfunctional pads and are not beneficial. Note: For mechanical mounting holes that are not plated, there is no need to place capture pads on the outer layers.

**Clearance hole-** the hole etched in a copper plane to allow a drilled hole to pass through. The hole may be plated or unplated.

**Hole shadow-** the shadow cast through all PCB layers by the drilled hole. Features in signal layers must be kept away from this “shadow” by a dimension corresponding to the insulation thickness required to meet appropriate standards. The hole shadow is defined by the diameter of the drilled hole and the worst case wander that the hole may have in the final PCB. This “wander” is composed of drilling inaccuracies, layer to layer registration inaccuracies, inaccuracies in the working artwork and shrinkage of the laminate layers from the heat of lamination. Because of hole wander, plated copper may be found out to the edge of the hole shadow. Therefore, insulation thickness must start at the hole shadow and extend outward in both power and signal layers.

**Manufacturing tolerance-** the dimension that describes how a drilled hole will wander out of its true position. The inaccuracy components are described in the hole shadow description.

**Hole plating-** the copper plating deposited in a hole to create a connection between signal pins and traces or power pins and power planes. This plating is deposited after the PCB has been laminated and drilled.

**Copper foil-** the outer layers of all PCBs are formed using copper foil. This foil serves as an electrical path to conduct the plating current needed to plate copper in the holes and on the pads and traces that will be present on the surfaces of the finished PCB. After the plating steps have been completed, the foil is etched to form the traces, pads and other outer layer features.

**Insulation gap-** the insulating material that exists between the hole shadow (copper plating in the hole) and metallic features in all of the layers. Examples are traces and planes.

**Annular ring-** the copper in the capture pad that extends past the drilled hole shadow. The capture pad is intentionally made larger than the drilled hole and the hole shadow in order to insure that there is always a portion of the pad making contact with the trace, even when the drilled hole is out of position due to drill tolerances.

**Plane-** any copper plane layer inside the PCB. Could be ground, Vdd or any other plane used to make electrical connections or to serve as partners for controlled impedance lines.

**Pad Stack-** the name given by CAD systems to describe the sizes of the capture pad, plane clearance, drill size and plating. The methods used to calculate these will be described in this document.

## IMPORTANT DIMENSIONS

**Finished hole diameter-** drill size minus copper plating.

**Drilled hole diameter-** finished hole diameter plus copper plating

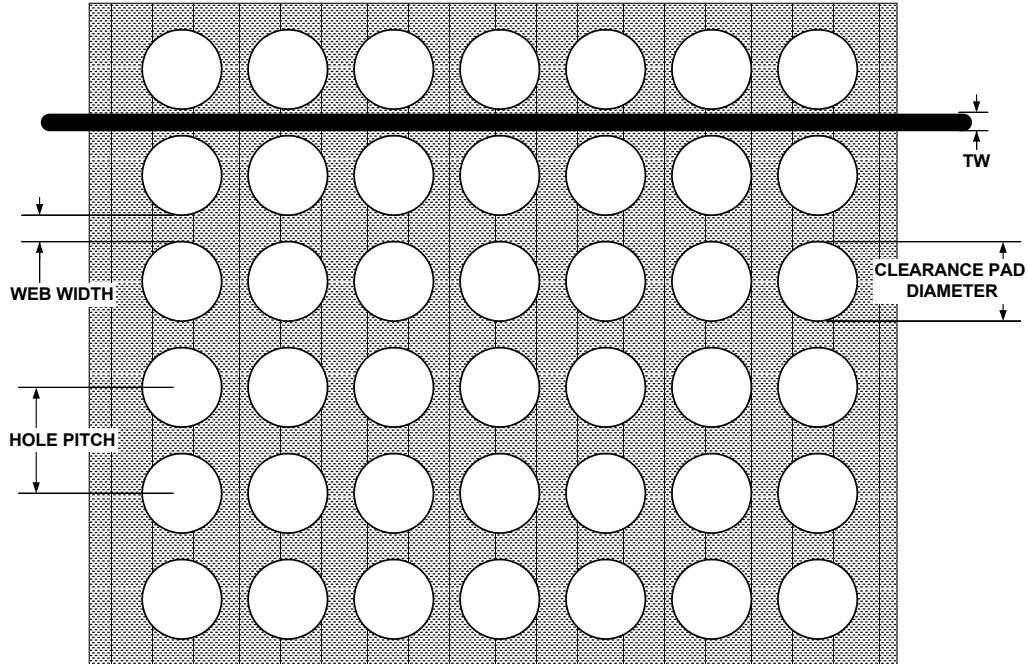
**Hole shadow-** drilled hole diameter plus manufacturing tolerance.

**Capture pad-** hole shadow plus annular ring allowance

**Clearance pad-** hole shadow plus insulation gap.

**Plane web**- the web of copper in a power plane between two clearance pads. See figure 2.

### TYPICAL HOLE PATTERN IN A POWER PLANE CAUSED BY A BGA OR PIN GRID ARRAY



**Figure 2. A Typical Hole Pattern Under a BGA.**

**Insulation gap**- on inner layers, the thickness of dielectric needed to separate copper features on the same layer from each other. This could be the distance between the plating of a plated through hole and the plane copper or the distance between the plating in a plated through hole and a trace in a trace layer. For most products this is 5 mils minimum.

When designing a pad stack for a hole, there are four main considerations. These are:

1. Insure that the pad used to connect a trace to the plating in a hole (capture pad) is large enough that the connection between the trace and the plating in the hole is always made with copper from the pad. When the connection is made only by the end of the trace to the plating (called a butt connection), this joint is weak and will fracture during soldering. The connection is assured by making sure the capture pad is larger than the hole shadow by enough to assure a solid connection. This is specified as a minimum annular ring. Normally this is 2 mils minimum per side. The condition where a hole wanders enough to create a butt connection is called "breakout".
2. Insure that the hole in the plane through which the hole passes is large enough that the distance between the plating in the hole (hole shadow) and the edge of the plane is large enough to meet the insulation requirements of the design. For almost all PCBs this will be 5 mils minimum.
3. Insure that the distance between the edge of a trace passing by a via in a signal layer is large enough to satisfy the insulation spacing specification. Usually hole shadow plus 5 mils per side. Note: traces must not pass closer to a plated through hole than the web width in the underlying plane. Therefore, the space in signal layers that can be used for signals is only as wide as the web between holes.
4. Insure that the web in the planes between adjacent holes is wide enough to provide good signal integrity for transmission lines passing over them. Note: when the trace is the same width as the plane web, the impedance will increase. In the case of a 5 mil, 50 ohm trace passing over a 5 mil web as shown in Figure 2, the impedance will increase to nearly 80 ohms. It can be shown that when the web increases to at least 1.5 times the trace width, impedance increases will be less than 5%.

## PAD STACK CALCULATIONS

The pad stack is made up of four components: finished or plated hole size, drilled hole size, capture pad size and clearance hole size. The following calculations result in the minimum sizes for all features. When possible, pad stacks should be designed with larger tolerances. The minimum size is required with 50 mil pitch and 1 mm pitch BGAs and fine pitch connectors in order to balance the tradeoffs between manufacturability and good signal integrity.

**Drilled hole size-** Finished hole size plus 3 mils for plating (1.5 mils per side) plus drill size tolerance. Drilled hole tolerance is  $\pm 1/2$  mil based on input from Procket's main suppliers. Because this is such a small error, it does not need to be included. The 12 mil manufacturing tolerance more than accounts for this.

**Hole Shadow Diameter-** Drilled hole size plus manufacturing tolerance. For 18" X 24" high layer count panels built by the top tier fabricators the manufacturing tolerance is 12 mils. For 16" X 18" panels built by the same fabricators the manufacturing tolerance is 10 mils.

**Capture Pad Diameter-** hole shadow plus 4 mils.

**Clearance Pad Diameter-** Hole shadow plus 10 mils.

When calculating the above dimensions for vias (holes that don't have leads soldered into them) the starting point is drill size, since the diameter of the finished hole is not important. The minimum drilled hole size that can be reliably plated in very high quantities is the starting point. For 100+ mil thick PCBs, this is 12 mils.

### Example calculation for 18" X 24" panel 100+ mil thick PCB:

Hole shadow = drill + 12 mils

Capture pad = drill + 12 mils + 4 mils = drill plus 16 mils.

Clearance pad = drill + 12 mils + 10 mils = drill + 22 mils.

The pad stack for a 12 mil drill is: capture pad = 28 mils, clearance pad = 34 mils.

Using the above data for 50 mil pitch BGAs and a 12 mil drill the plane web will be  $50 - 34$  mils = 16 mils.

Using the above data for 1 mm pitch BGAs (39.7 mil pitch) and a 12 mil drill the plane web will be  $39.7 - 34 = 5.7$  mils.

### Example calculation for 16" X 18" panel 100+ mil thick PCB

Hole shadow = drill + 10 mils

Capture pad = drill + 10 mils + 4 mils = drill plus 14 mils

Clearance pad = drill + 10 mils + 10 mils = drill + 20 mils

The pad stack for 12 mil drill is: capture pad = 26 mils, clearance pad = 32 mils.

Using this data for 50 mil pitch BGAs and 12 mil drill the plane web will be  $50 - 32 = 18$  mils

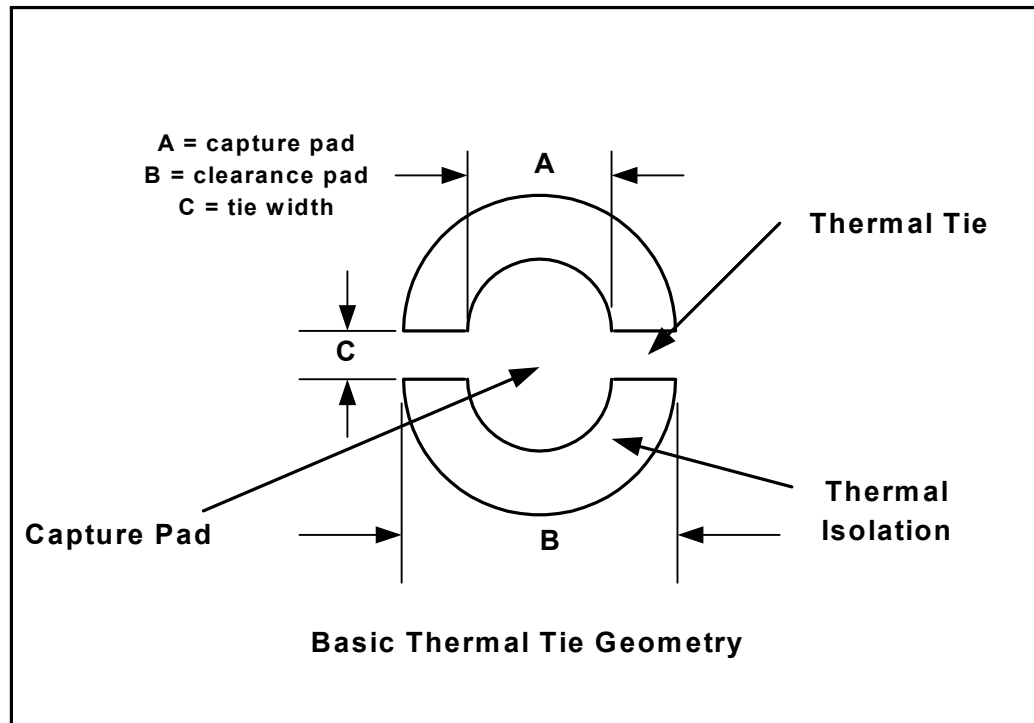
Using the above data for 1 mm pitch BGAs (39.7 mil pitch) and a 12 mil drill the plane web will be  $39.7 - 32 = 7.9$  mils.

## UNPLATED HOLES

An unplated hole is usually used for mounting hardware that is not intended to make connections to any of the circuits on the PCB. When calculating the pad stack for an unplated hole, there will be no capture pads on inner or outer layers. The only calculation will be for the clearance pads that are etched in the power planes to allow the hole to pass through. This calculation is the same as for a plated hole.

## THERMAL TIES

When a plated through hole is used to connect the power pins of leaded components to the internal power planes of a PCB the planes will “sink” away the heat needed to solder and unsolder the component. As a result, it may be impossible install or remove components. To solve this problem it is necessary to provide some thermal isolation between the plated through hole and the plane. This is done with narrow “ties” or thermal ties between the plated through hole and the plane. See Figure 3.



**Figure 3, Thermal Tie Design**

The capture pad, A, above need only be the size of the hole shadow. (drill + mfg. tolerance) The breakout problem is solved by placing two ties on opposite sides of the capture pad. The clearance pad is calculated the same as for any via (drill + mfg. tol + insulation.)

Thermal ties are not needed to connect the power leads of surface mount components to planes and should not be used.

For a full discussion of thermal ties, both electrical and thermal, see the paper listed at the end of this document.

References: Power Plane Thermal Tie Design, By Lee Ritchey, Feb 16, 2001.d