# 2102-545 Digital ICs 

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## Assignment \#1 Solution

## Problem 1: Cost Analysis of Microprocessors

(A) To find the number of good chips per wafer, we need to know the number of dies per wafer and the die yield, which can be computed using the equations in the lecture. Note that the equations to compute the die yield is modified by the wafer yield. The wafer yield accounts for the fact that not all wafers are good to start with. A wafer yield of $95 \%$ means, on average, 5 in 100 wafers delivered to the fabrication plants do not pass parameter testing.

$$
\begin{aligned}
& \text { Dies per wafer }=\frac{\pi \times(\text { Wafer diameter } / 2)^{2}}{\text { Die area }}-\frac{\pi \times \text { Wafer diameter }}{\sqrt{2 \times \text { Die area }}} \\
& \text { Die yield }=\text { Wafer yield } \times\left(1+\frac{\text { Defects per unit area } \times \text { Die area }}{\alpha}\right)^{-\alpha} \\
& \text { Number of good chips per wafer }=\text { Dies per wafer } \times \text { Die Yield }
\end{aligned}
$$

Calculation Example: Alpha 21264C with defect density $=0.5 \mathrm{~cm}^{-2}$, wafer yield $=$ $95 \%$ and $\alpha=4$.

$$
\begin{gathered}
\text { Dies per wafer }=\frac{\pi \times(20 \mathrm{~cm} / 2)^{2}}{115 \mathrm{~mm}^{2}}-\frac{\pi \times 20 \mathrm{~cm}}{\sqrt{2 \times 115 \mathrm{~mm}^{2}}} \cong 231 \text { (rounded down) } \\
\text { Die yield }=0.95 \times\left(1+\frac{0.5 \mathrm{~cm}^{-2} \times 115 \mathrm{~mm}^{2}}{4}\right)^{-4}=0.555
\end{gathered}
$$

Number of good chips per wafer $=231 \times 0.555 \cong 128$ (rounded down)

Results for the other microprocessors can be found in table 1.1.
(B) The cost per projected good dies can be found by dividing wafer cost by number of expected good chips per wafer, which have already been calculated in part(a).

$$
\text { Die Cost }=\frac{\text { Wafer Cost }}{\text { Dies per wafer } \times \text { Die Yield }}=\frac{\text { Wafer Cost }}{\text { Number of good chips per wafer }}
$$

Calculation Example (continued): Alpha 21264C with defect density $=0.5 \mathrm{~cm}^{-2}$, wafer yield $=95 \%$ and $\alpha=4$.

$$
\text { Die Cost }=\frac{\$ 4700}{128}=\$ 36.72
$$

Results for the other microprocessors can be found in Table 1.1.
(C) Cost of a processor depends on three components: die cost, die testing cost, and package cost. Die cost is known from part (b). Die testing cost can be computed using the equation given in the assignment. Package cost varies with the technology selected, indicated in table 1.34 for each processor. The packaging costs of various technologies are given in figure 1.35.

$$
\begin{gathered}
\text { Cost of testing die }=\frac{\text { Cost of testing per hour } \times \text { Average die test time }}{\text { Die yield }} \\
\text { Cost of integrated circuit }=\frac{\text { Die Cost }+ \text { Cost of testing die }+ \text { Cost of packaging }}{\text { Final test yield }}
\end{gathered}
$$

Calculation Example (continued): Alpha 21264C chip with 524-pin CLGA.

$$
\begin{gathered}
\text { Die Cost }=\$ 36.72(\text { from part }(\mathrm{b})) \\
\text { Cost of testing die }=\frac{\$ 440 \times(25 \mathrm{sec} / 3600 \mathrm{sec} \text { per hr })}{0.555}=\$ 5.50
\end{gathered}
$$

Cost of packaging = \$25 (from figure 1.35)

$$
\text { Cost of a good Alpha21264C chip }=\frac{\$ 36.72+\$ 5.50+\$ 25}{100 \%}=\$ 67.22
$$

Results for the other microprocessors can be found in Table 1.1.

Table 1.1: Results for part (a) - (c)

| Microprocessors | Die Area $\left(\mathrm{mm}^{2}\right)$ | Pin | Wafer cost | Package | Dies per wafer | Die yield | No. good chips/ wafer | Die Cost | Testing Cost | Package Cost | Cost of Microprocessors |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Alpha 21264C | 115 | 524 | \$4,700 | CLGA | 231 | 0.555 | 128 | \$36.72 | \$5.50 | \$25 | \$67.22 |
| Power3-II | 163 | 1088 | \$4,000 | SLC | 157 | 0.452 | 71 | \$56.34 | \$5.16 | \$20 | \$81.50 |
| Itanium | 300 | 418 | \$4,900 | PAC | 79 | 0.266 | 20 | \$245.00 | \$12.54 | \$20 | \$277.54 |
| MIPS R14000 | 204 | 527 | \$3,700 | CPGA | 122 | 0.383 | 46 | \$80.43 | \$7.98 | \$25 | \$113.41 |
| UltraSPARC III | 210 | 1368 | \$5,200 | FC-LGA | 118 | 0.374 | 44 | \$118.18 | \$10.70 | \$30 | \$158.88 |

(D) The largest microprocessor in terms of area is the Intel's Itanium. By repeating part (a) to (c), the cost of a good Itanium chip can be found for defect densities of 0.3 and 1 defects per cm . The results are summarized in table 1.2.

Table 1.2: Cost effect due to increase in defects

| Microprocessors | Dies per <br> wafer | Die yield | No. good <br> chips/ wafer | Die Cost | Testing <br> Cost | Package <br> Cost | Cost of <br> Microprocessors |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Itanium @ 0.3 defects/cm ${ }^{2}$ | 79 | 0.422 | 33 | $\$ 148.48$ | $\$ 7.90$ | $\$ 20$ | $\$ 176.39$ |
| Itanium @ 1 defects $/ \mathrm{cm}^{2}$ | 79 | 0.101 | 8 | $\$ 612.50$ | $\$ 32.91$ | $\$ 20$ | $\$ 665.41$ |

From the table, we see that increase in defect density has a drastic effect on the final cost of a microprocessor. This effect is more pronounced in a larger processor due to a sharp reduction of the total yield. The bigger the die area of a microprocessor the more likely the die will be corrupted by the defects. (You just need only one defect to fail an IC!)
(E) For the Alpha 21264C with six levels of metal interconnect, the cost of a good (i.e., working, packaged, and tested) die when $\alpha=4$ and $\alpha=6$ can be found by repeating part (a) to (c), assuming that the defect density is 0.8 defects per cm . The results are summarized in table 1.3.

Table 1.3: Cost effect due to change in $\alpha$

| Microprocessors | Dies per <br> wafer | Die yield | No. good <br> chips/ wafer | Die Cost | Testing <br> Cost | Package <br> Cost | Cost of <br> Microprocessors |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Alpha 21264C @ $\alpha=4$ | 231 | 0.415 | 95 | $\$ 49.47$ | $\$ 7.36$ | $\$ 25$ | $\$ 81.84$ |
| Alpha21264C @ $\alpha=6$ | 231 | 0.404 | 93 | $\$ 50.54$ | $\$ 7.57$ | $\$ 25$ | $\$ 83.11$ |

From the table, we see that increase in process complexity results only in a slight increase in the final cost. This is why later generations of technology usually provide many levels of metal interconnect. The price you pay for improved routeability is quite inexpensive.

