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MILITARY STANDARD

PRINTED WIRING FOR ELECTRONIC EQUIPMENT

DEPARTMENT OF DEFENSE
Washington, DC 20301

Printed Wiring for Electronic Equipment

MIL-STD-275E

1. This Military Standard is approved for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Naval Electronic Systems Command, ATTN: ELEX-8111, Washington, DC 20363, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document, or by letter.

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FIGURES

1. SCOPE

1.1 Purpose. This standard establishes design requirements governing rigid, single-sided printed-wiring boards, double-sided printed-wiring boards, multilayered printed-wiring boards, printed-wiring assemblies constructed from those boards mentioned above, and design considerations for the mounting of parts and assemblies thereon. The design criteria (such as electrical spacings) contained in this standard are predicated on the requirement that end item assemblies (circuit card assemblies, printed-wiring assemblies, back planes, mother boards) shall be conformally coated (see 6.3.1). Conformal coating shall be in accordance with MIL-I-45058.

1.2 Classification. Printed-wiring boards shall be of the types shown, as specified (see 4.2):

Type 1 - Single-sided board
Type 2 - Double-sided board
Type 3 - Multilayer board

2. REFERENCED DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. Unless otherwise specified, the following specifications, standards, and handbooks, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards (DoDISS) specified in the solicitation, form a part of this standard to the extent specified herein.

SPECIFICATIONS

FEDERAL

L-F-340	-	Film, Sensitized, Wash-Off Process, Diazotype, Moist and Dry Process, Brownprint, Roll and Sheet.
QQ-B-626	-	Brass, Leaded and Nonleaded Rod, Shapes, Forgings and Flat Products with Finished Edges (Bar, Flat Wire and Strip).
QQ-B-750	-	Bronze, Phosphor Bar, Plate, Rod, Sheet, Strip, Flatwire, and Structural and Special Shaped Sections.
QQ-C-576	-	Copper Flat Products with Slit, Slit and Edge-Rolled, Sheared, Sawed, or Machined Edges, (Plate, Bar, Sheet, and Strip).
QQ-N-290	-	Nickel Plating (Electrodeposited).
QQ-S-571	-	Solder; Tin Alloy; Lead-Tin Alloy; and Lead Alloy.

MILITARY

MIL-D-8510	-	Drawings, Undimensioned, Reproducibles, Photographic and Contact, Preparation of.
MIL-P-13949	-	Plastic Sheet, Laminated, Metal-Clad (For Printed Wiring), General Specification for.
MIL-C-14550	-	Copper Plating (Electrodeposited).
MIL-P-28809	-	Printed-Wiring Assemblies.
MIL-G-45204	-	Gold plating, Electrodeposited.
MIL-I-46058	-	Insulating Compound, Electrical (For Coating Printed Circuit Assemblies).
MIL-P-55110	-	Printed-Wiring Boards.
MIL-P-81728	-	Plating, Tin-Lead, Electrodeposited.

STANDARDS

MILITARY

DOD-STD-100	-	Engineering Drawing Practices.
MIL-STD-130	-	Identification Marking of U.S. Military Property.
DOD-STD-1686	-	Electrostatic Discharge Control Program For Protection of Electrical and Electronic Parts, Assemblies and Equipment.

(Copies of specifications, standards, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Other publications. The following documents form a part of this standard to the extent indicated herein. The issues of the documents which are indicated as DOD adopted shall be the issue listed in the current DoDISS and the supplement thereto, if applicable.

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI-Y14.5	-	Dimensioning and Tolerancing for Engineering Drawings.
ANSI-Y14.1	-	Drawing Sheet Size and Format

(Application for copies should be addressed to the American National Standards Institute, Inc., 1430 Broadway, New York, NY 10018.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM - E53 - Standard Method for Chemical Analysis of Copper (Electrolytic Determination of Copper).

(Application for copies should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE-STD-200(ANSI Y32.16) - Reference Designations for Electrical and Electronic Parts and Equipments.

(Application for copies should be addressed to Institute of Electrical and Electronics Engineers Service Center, ATTN: Publication Sales, 445 Hose Lane, Piscataway, NJ 08854.)

INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS (IPC)

IPC-T-50 - Terms and Definitions.
IPC-CF-150 - Copper Foil for Printed Wiring Applications.
IPC-D-350 - End Product Description in Numeric Form.
IPC-S-815 - General Requirements for Soldering Electronic Interconnections.
IPC-SM-840 - Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards.

(Application for copies should be addressed to the Institute for Interconnecting and Packaging Electronic Circuits, 3451 Church Rd., Evanston, IL 60203.)

2.3 Order of precedence. In the event of a conflict between the text of this standard and the references cited herein, the text of this standard shall take precedence.

4. GENERAL REQUIREMENTS

4.1 Design features. The design features of the printed-wiring boards shall be in accordance with this standard. Quality conformance test circuitry shall also be included on the production master. Quality conformance test circuitry shall be included on each panel and shall be in accordance with figure 1 and 5.9. Test circuitry shall be not more than 0.5 inch (13 mm) and shall be not less than 0.25 inch (6.4 mm) from the edge of the printed board, and represents all the manufacturing processes such as drilling, plating, etching, fusing, ground/voltage/ thermal/mechanical planes or cores, separately fabricated layers, permanent coatings (solder mask) and so forth.

4.2 Documentation. Requirements for drawing content may be satisfied by direct delineation on the drawing or by reference to other documents which are part of the engineering drawing set (see figure 2.).

4.2.1 Reference designations. Reference designations of components to be mounted on printed-wiring boards, when specified on the master drawing or the printed-wiring assembly drawing, shall be in accordance with IEEE-STD-200.

4.2.2 Deviation request and approval. When a deviation to this standard is necessary, or has been granted in the initial contract design description, the contractor (before proceeding further) shall furnish each proposed master drawing, or a detailed deviation request to the Government Agency concerned for approval with justification for the deviation. If approved, all deviations granted shall be documented on the master drawing.

4.2.3 Government furnished master drawings. Any deviation from this standard or drawing shall have been recorded on the Government approved master drawing or a Government approved deviations list. When new or additional deviations from this standard or drawing are necessary, the contractor (before processing further) shall furnish one copy of each proposed master drawing being revised, or a detailed deviation request to the Government Agency concerned for approval with justification for the deviation. If approved, all deviations granted shall be documented on the master drawing or the Government approved deviations list.

4.2.4 Conflicts. In the event of any conflict between the approved master drawing supplemented by an approved deviation list, if applicable, and the requirement of this standard, the approved master drawing and deviations list shall take precedence.

4.3 Master drawing. The master drawing shall be prepared in accordance with DOD-STD-100; shall include all appropriate detail board requirements (see section 5), and the following:

a. The type, size, and shape of the printed-wiring board.
b. The size, location, and tolerance of all holes therein.
c. Etchback allowances, when required or permitted.
d. Location of traceability marking.
e. Dielectric separation between layers.
f. Shape and arrangement of both conductors and nonconductor patterns defined on each layer of the printed-wiring board. Copies of the production masters or copies of the artwork may be used to define these patterns.
g. Separate views of each conductor layer.
h. Any and all pattern features not controlled by the hole sizes and locations shall be dimensioned either specifically, or by reference to the grid system (see n).
i. Processing allowances that were used in the design of the printed-wiring board (see 5.1.1, 5.1.4, 5.2.1.2, 5.2.2, and 5.2.2.6).
j. All notes either included on the first sheet(s) of the master drawing or by specifying the location of the notes on the first sheet.
k. Conductor layers numbered consecutively starting with the component side as layer 1. If there are no conductors or lands on the component side, the next layer shall be layer 1. For assemblies with components on both sides, the most densely populated side shall be layer 1.

l. Identification marking (see 5.8).
m. Size, shape, and location of reference designation and legend markings, if required (see h).
n. A modular grid system to identify all holes, test points, lands, and overall board dimensions with modular units of length of 0.100, 0.050, 0.025, or other multiples of 0.005 inch in that order of preference. For design where the majority component locations are metric-based (SI), the basic modular units of length shall be 2.0, 1.0, 0.5, or other multiples of 0.1 mm in that order of preference. The grid system shall be applied in the X and Y axes of the Cartesian coordinates. The grid shall not be reproduced on the master drawing; but may be indicated using grid scales or X, Y control dimensions (see figure 3).
o. Dimensions for critical pattern features which may effect circuit performance because of distributed inductance or capacitance effects within the tolerance required for circuit performance.
p. All terms used on the master drawing shall be in conformance with the definitions of ANSI/IPC-T-50 or ANSI Y14.5 (see 3.1 and 2.2).
q. Deviations to this standard (see 4.2.2).
r. Minimum line width and spacing of the finished printed-wiring board.
s. Maximum rated voltage (maximum voltage between the two nonconnected adjacent conductors with the greatest potential difference) for type 3 boards only.
t. Plating and coating material(s) and thickness(es).
u. Identification of test points required by the design (see 5.1.8).
v. Applicable fabrication specification with date(s), revision letter, and amendment number.

When continuation sheets of a drawing are used for conductor pattern definition, they need not be prepared on standard drawing forms provided standard sheet sizes are used with standard continuation sheet title blocks in accordance with ANSI Y14.1 located in the lower right corner of each sheet. Numeric form of end product descriptions shall be in accordance with IPC-D-350.

4.3.1 Hole location tolerance. Unless otherwise specified, the location of holes shall be dimensioned with respect to single or secondary grid systems. Each distinctive hole pattern (such as, plated-through holes, tooling holes, mounting holes, windows, access holes, and so forth), may require separate consideration or specification of tolerance. Producibility considerations are presented in table VI.

4.3.2 Processing allowances. The processing allowances which were considered in the design and artwork preparation for the printed-wiring board shall be documented and defined on the master drawing in either note form or by reference to another drawing which contains artwork requirements or specifications. This information shall be expressed in terms of the maximum variation between the end-product conductor widths and spacings and what may appear on the artwork; the minimum land, in reference to the drilled or plated hole and what may appear on the artwork; or any other feature conditions considered in the design where the variation between end-product and artwork configuration play a role in the producibility of the printed-wiring board.

4.3.3 Datums. There shall be a minimum of two datum features to establish the mutually perpendicular datum reference frame for each board. These datums shall be established by at least two holes, points, symbols, or other datum features, but not edges. Critical design features may require the use of more than one set of datum references. The master drawing shall establish the relationship and acceptable tolerance between all datums features. All datum features shall be located on grid or establish grid criterion, as defined on the master drawing, and should be on or within the outline of the printed-wiring boards.

4.4 Printed-wiring assembly drawing. The printed-wiring assembly drawing shall cover printed-wiring on which separately manufactured parts have been added. The printed-wiring assembly drawing shall be in accordance with DOD-STD-100 and should include at least the following:

a. Parts and material list.
b. Component mounting and installation requirements.
c. Cleanliness requirements per MIL-P-28809.
d. Location and identification of materials or components (or both).
e. Component orientation and polarity.
f. Applicable ordering data from MIL-P-28809.
g. Structural details when required for support and rigidity.
h. Electrical test requirements.
i. Marking requirements.
j. Electrostatic discharge protection requirements.
k. Special solder plug requirements.
l. Eyelets and terminals.
m. Lead forming requirements.
n. Type of conformal coating and masking.
o. Solder mask.
p. Traceability.

The printed-wiring assembly drawing shall include the definition of any conditions considered in the design where the manufacturing variation between the end product and assembly configuration play a role in the producibility or performance of the printed-wiring assemblies.

4.4.1 Deviation request and approval. When a deviation to this standard is necessary, or has been granted in the initial contract design description, the contractor (before proceeding further) shall furnish each proposed assembly drawing, or a detailed deviation request to the Government Agency concerned for approval with justification for the deviation. If approved, all deviations granted shall be documented on the assembly drawing.

4.4.2 Government furnished assembly drawings. Any deviation from this standard or the drawing shall have been recorded on the Government approved assembly drawing or a Government approved deviations list. When new or additional deviations from this standard or the drawing are necessary, the contractor (before proceeding further) shall furnish one copy of each proposed assembly drawing being revised, or a detailed deviation request to the Government Agency concerned for approval with justification for the deviation. If approved, all deviations granted shall be documented on the assembly drawing or the Government approved deviations list.

4.4.3 Conflicts. In the event of any conflict between the approved assembly drawing supplemented by an approved deviation list, if applicable, and the requirement of this standard, the approved assembly drawing and deviations list shall take precedence.

4.5 Production master. When specified in the contract or purchase order, a production master of each layer shall be provided as part of the drawing set. When a production master is not supplied, the manufacturer shall be responsible for the preparation of the production master with sufficient accuracy to meet the requirements of the printed wiring detailed on the master drawing. The production master shall be as defined in IPC-T-50 and shall be supplied or prepared on 0.0075 ±0.0005 inch thick biaxially oriented, dimensionally stable polyester type film or equal, in accordance with MIL-D-8510, type II; L-F-340 film, photographic subclass a, class 2, type I or II, style 1A or photographic glass plates. The accuracy of the production master (single image, multiple image, or any associated quality assurance coupons) shall be such that the lands, conductors, and other features shall be located within 0.004 inch diameter of the true grid position established for the layer, and that for the composite production master, the features of all layers shall coincide within 0.006 inch diameter of the true grid position, when measured at 20°C ±1°C, and 50 ±5 percent relative humidity after the material has stabilized. In the event that tighter tolerances are required in order to produce printed wiring, the production master precision requirements as considered in the design process, shall be defined on the master drawing.

5. DETAIL BOARD REQUIREMENTS

5.1 Conductor pattern.

5.1.1 Conductor thickness and width. The width and thickness of conductors on the finished printed-wiring board shall be determined on the basis of the current carrying capacity required. The temperature rise shall be determined in accordance with figure 4a for type 1, type 2, and external layers of type 3 boards, and figure 4b for internal layers of type 3 boards. For ease of manufacture and durability in usage conductor width and spacing requirements shall be maximized while maintaining the minimum spacing requirements of table I. The minimum conductor width shown on the master drawing shall be not less than 0.004 inch (0.10 mm). To maintain the conductor width shown on the master drawing, the line widths on the production master shall be compensated for process allowances as shown in 20.1 and table VI of the appendix.

5.1.2. Conductors with less than 90° included angle. All conductors that change direction where the included angle is less than 90° shall have the external corners of the conductor rounded.

5.1.3 Conductors. The length of a conductor between any two lands should be held to a minimum. However, conductors which are straight lines and run in X, Y, or 45° directions in general are preferred to aid computerized documentation for mechanized or automated layouts.

5.1.4 Conductor spacing. Larger spacings shall be used whenever possible and the minimum spacing between conductors, between conductor patterns, and between conductive materials (such as conductive markings or mounting hardware) and conductors shall be in accordance with table I, and defined on the master drawing. To maintain the conductor spacing shown on the master drawing, space widths on the production master shall be compensated for process allowances as shown in 20.1 and table VI of the appendix. Plated-through holes passing through internal foil planes (ground and voltage) and thermal planes shall meet the same minimum clearance between the plated-through hole and foil or ground planes as required for spacing between internal conductors.

TABLE I. Conductor spacing.

Voltage between conductors DC or AC peak (volts)	Minimum spacing	
	Surface layers	Internal layers
0-100	0.005 inch (0.13 mm)	0.004 inch (0.10 mm)
101-300	0.015 inch (0.38 mm)	0.008 inch (0.20 mm)
301-500	0.030 inch (0.76 mm)	0.010 inch (0.253 mm)
Greater than 500 1/	0.00012 inch (.00305 mm) per volt	0.0001 inch (.0025 mm) per volt

1/ For reference only, voltages greater than 500 should be evaluated for the specific design application.

5.1.5 Edge spacing. The minimum spacing between conductive patterns and the edge of the printed-wiring board or any adjacent conductive surface, such as supporting structure or frames (nonmoving), shall be not less than the minimum spacing specified in table I plus .015-inch (0.38 mm), provided the edges are protected from physical harm in the installed assembly configuration. Printed wiring not so protected shall have a minimum conductor to edge distance of 0.050 inch (1.25 mm). The edge spacing requirement is not applicable to heat sinks and ground planes. To maintain the edge spacing shown on the master drawing, the edge spacings shall be compensated for process allowances as shown in 20.1 and table VI of the appendix.

5.1.6 Large conductive areas. Large conductive areas increase the likelihood for blistering or bowing during the soldering operation. The pattern and location of large conductive areas should be per 5.1.6.1 and 5.1.6.2. Design of conductive areas should provide balanced construction and include the use of nonfunctional copper, if practical.

5.1.6.1 Large external conductive areas. External conductive areas that extend beyond a 1-inch diameter circle should contain etched areas that will break up the large conductive area but will retain the continuity and functionality of the conductor. If etched areas are not provided, other methods should be used to minimize blistering or bowing. Large conductive areas should, if possible, be on the component side of the board. If solder mask is employed, over melting metals, conductive areas larger than 0.050 inches wide shall not be employed under the solder mask, see IPC-SM-840 and 20.5 of the appendix.

5.1.6.2 Large internal conductive areas (type 3). When a conductive area that extends beyond a 1-inch diameter circle is used on an internal layer, the layer should be placed as near the center of the board as possible and should contain etched areas that will break up the large conductive area but will retain the continuity and functionality of the conductor. If more than one internal layer has a large conductive area, the layers should be located in the board to provide balanced construction. For surface preparation considerations see 20.5 of the appendix.

5.1.7 Interfacial connections. Interfacial connections on type 2 and 3 printed-wiring boards shall be made by use of plated-through holes only. Wires, standoff terminals, eyelets, rivets, or pins shall not be used to provide interfacial connections.

5.1.7.1 Solder fillets and plugs. Printed-wiring boards subjected to wave or dip soldering shall be designed to facilitate flow of solder around component leads in plated-through holes and into plated-through holes without leads, so as to create a solder plug. Careful consideration shall be given to hole-to-lead diameter clearance (see 5.3.2 and 5.5) hole to board thickness ratios and heat relief of metal planes to promote solder plugging. In the event solder plugging due to natural capillary action is not possible, such as when a heat sink is bonded directly over plated-through holes, the design shall include provision for prevention of solder, flux or other chemicals from entering the plated-through hole. Solder may be prevented from entering the holes by prefilling these holes with an appropriate polymer plug, covering the holes with a sheet of permanent bonded material, tenting the holes with a permanent solder mask or blocking these holes with some temporary technique that will prevent solder access to the hole. All techniques must have sufficient durability to not break up when exposed to the solder process. The printed-wiring assembly drawing shall define the absence of such solder plug requirements. As a minimum solder plugs shall be required in:

a. All electrically functional and nonfunctional plated-through holes with a lead; the lead is required to be surrounded 360° by the solder plug no matter what technique for soldering is used.
b. Any plated-through hole without a lead, that is subject to wave or dip soldering with the degree and percentage of hole plugging described by the appropriate assembly or soldering specification (MIL-P-28809, IPC-S-815).

Solder plugs are not necessarily required in:

a. Any unsupported hole without a lead.
b. Nonfunctional plated-through holes (hand soldered or vapor phase reflowed assembly).
c. Any electrically functional plated-through hole (without a lead) not subjected to wave or dip soldering.
d. Any plated-through hole covered with permanent solder mask, other polymeric cover layer (not conformal coating) or is already filled with an appropriate polymer in order to prevent hole access during wave or dip soldering.
e. Any plated-through hole, electrically functional or not, without a lead, where access to the hole is limited by components, heat sinks, by design (blind vias), or where access of solder to the hole is prevented during the solder process.

5.1.8 Test points. When required by the design, test points for probing shall be provided as part of the conductor pattern and shall be identified on the master drawing and the assembly drawing. These "probe points" shall require that a land be available for probing as opposed to a conductor. Vias or component lead mounting lands may be considered as probe points provided that sufficient area is available for probing and maintaining the integrity of the via or component lead mounting joint. Probe points shall meet the plating requirements of 5.5.4.

5.2 Lands. Lands shall be provided for each point of attachment of a part lead or other electrical connection to the printed-wiring board.

5.2.1 Lands for through hole attachment. When through hole attachment is required, all of the requirements of 5.2 shall be considered in the design of the printed-wiring board except where 5.2.2 applies for surface attachment.

5.2.1.1 Lands location. The lands shall completely surround and abut on the mounting holes except where 5.2.2 and 5.2.6 applies.

5.2.1.2 Through hole land area requirements. The minimum diameter of the land surrounding an unsupported hole shall be at least 0.040 inch (1.02 mm) greater than the maximum diameter of the hole. When eyelets or standoff terminals are used, the lands on type 1, type 2, and external layers of type 3 boards shall be so designed as to have a minimum diameter of at least 0.020 inch greater than the maximum diameter of the projection of the eyelet or standoff terminal flange. The minimum diameter of a land surrounding a plated-through hole on type 2 and type 3 boards shall be determined by considering the following:

a. Maximum diameter of the drilled hole.

b. Minimum annular ring requirements (see 5.2.3). Etchback, when required, will reduce the insulation area that supports the internal land. The minimum annular ring considered in the design shall be not less than the maximum etchback allowed.
c. A standard fabrication allowance, determined by statistical survey, which considers production master tooling and process variations required to fabricate boards (see table II).

TABLE II. Minimum standard fabrication allowances for plated-through hole attachment.

Greatest board/panel dimension	Preferred inches	Standard inches	Reduced producibility inches
Up to 12 inches	0.028	0.020	0.012 1/
More than 12 inches	0.034	0.024	0.016 1/

The above considerations shall be incorporated into the minimum land area provided on the production master such that: Minimum land diameter = a+2b+c. All lands and annular rings shall be maximized wherever feasible, consistent with good design practice and electrical clearance requirements.

1/ For copper weights greater than 1 oz/sq.ft., add 0.002 inch minimum to the fabrication allowance for each additional oz/sq.ft. of copper used.

5.2.2 Lands for surface attachment. When surface attachment is required, all of the requirements of 5.2 shall be considered in the design of the printed-wiring board except where 5.2.1 and 5.2.6 apply. The selection, design, and position of the land geometry in relation to the part may significantly impact the solder joint. The designer must understand the capabilities and limitations of the manufacturing and assembly operations.

5.2.2.1 Lands for end-capped discrete components. Discrete components, when mounted as defined in 6.2.12.3, shall have their land relationships identified as shown on figure 5.

5.2.2.2 Land pattern for leadless chip carriers. The attachment lands for surface mounting leadless chip carriers should be the same width as the component terminal (castilation maximum) plus 0.005 inch (0.01 mm) whenever possible. The land length should extend between 0.015 inch to 0.04 inch (0.38 to 1.02 mm) beyond the maximum chip carrier outline on all four sides to create a horizontal solder fillet length equal to the vertical fillet rise (see figure 6). The design of fan-out to interconnect the basic land pattern to other circuitry/devices is dependent on wiring density, testability, assembly, repairability, and routability requirements. Figure 7 shows some examples of possible fan-out patterns for leadless chip carriers. Chip carrier land sites should be located on a fixed grid within the printed board to optimize testing. This grid should be compatible with assembly and testing equipment so as to minimize the amount of specialized and complex equipment necessary.

5.2.2.3 Lands for leaded chip carriers. The land size for ceramic and for leaded chip carriers should match the lead configurations. J shaped leads should have the land width be equal to or 0.005 inch larger than the width of the lead. The land length should extend between 0.015 inch to 0.040 inch (0.38 to 1.02 mm) beyond both sides of the foot of the J pattern. Other types of leads used for chip carriers should have the land commensurate with the lead configuration, in order to create a horizontal solder fillet length at the toe and heel of the lead configuration, as shown on figure 8.

5.2.2.4 Lands for ribbon leaded surface mounted parts. The land requirements for mounting ribbon leaded parts, such as "flat packs", "quad packs", or small outline devices, shall preferably be rectangular. The minimum land width shall be equal to or exceed the maximum lead width by the amount shown on figure 8 providing room for both solder fillets at both the heel and toe of the ribbon lead. The minimum land width shall be approximately one and one-half times the width of the lead, or 0.005 inch (0.13 mm), whichever is less (see figure 9). Flat pack termination shall be staggered to permit greater spacing wherever possible. The center position of ribbon leaded components should be on a fixed grid, wherever possible, to facilitate testing.

5.2.2.5 Lands for flattened round leads. Flattened round leads shall have a land which will provide the seating so that the heel and the terminal relationship is in accordance with figure 10. Leads shall be seated with no side overhang. Toe overhang is acceptable, provided that the flattened lead in contact with the terminal area is a minimum of 150 percent of the unflattened lead diameter and the overhang does not reduce the spacing to adjacent parts to less than that specified on the assembly drawing.

5.2.2.6 Lands for plated-through holes (vias for boards with surface attached parts). The minimum diameter of a land surrounding a plated-through hole on type 2 and type 3 boards where surface attachment is used shall be determined by considering the following:

a. Maximum diameter of the drilled hole.
b. Minimum annular ring (see 5.2.3). Etchback, when required, will reduce the insulation that supports the internal land. The minimum annular ring considered in the design shall be not less than the maximum etchback allowed.
c. A standard fabrication allowance, determined by statistical survey, which considers tooling production master and process variations required to fabricate boards (see table III).

TABLE III. Minimum standard fabrication allowances for surface attachment.

Greatest board/panel dimension	Preferred inches	Standard inches	Reduced producibility inches
Up to 12 inches	+0.026	+0.018	+0.010 1/
More than 12 inches	+0.032	+0.022	+0.014 1/

The above considerations shall be incorporated into the minimum land provided on the master pattern such that: Minimum land diameter = a+2b+c. All lands and annular rings shall be maximized wherever feasible, consistent with good design practice and electrical clearance requirements.

1/ For copper weights greater than 1 oz/sq.ft., add 0.002 inch minimum to the fabrication allowance for each additional oz/sq.ft. of copper used.

5.2.3 Annular ring considerations. The minimum annular ring on external layers is the minimum amount of copper (at the narrowest point) between the edge of the hole and the edge of the land after plating of the hole. The minimum annular ring on internal layers is the minimum amount of copper (at the narrowest point) between the edge of the drilled hole and the edge of the land after drilling the hole.

External - The minimum annular ring for an unsupported hole shall be 0.015 inch. The minimum annular ring for a plated-through hole in type 2, and external layers of type 3 boards shall be 0.002 inch, except where the conductor joins the land the annular ring shall be 0.005 inch minimum (see figures 11 and 13).

Internal - The minimum annular ring for internal lands on type 3 boards shall be 0.002 inch (see figure 12). Etchback, when required, will reduce the insulation supporting the annular ring of internal lands. The minimum annular ring considered in the design shall be not less than the maximum etchback allowed.

5.2.4 Nonfunctional lands (type 3, internal layers). Nonfunctional lands may be included on internal layers of type 3 boards. They need not be used where electrical clearance requirements do not permit, such as, ground planes, voltage planes and thermal planes. Plated-through holes passing through internal foil planes (ground and voltage) and thermal planes shall meet the same minimum spacing requirements as that for conductors on internal layers (see table I).

5.2.5 Thermal relief in conductor planes. Thermal relief is only required for holes that are subject to soldering. Connections asspciated with large conductor areas (ground planes, voltage planes, thermal planes, etc.) shall have a land that is relieved locally in the area of the plated-through hole connection in a manner similar to that shown on figure 14. When electrical considerations preclude the use of this technique, approval to deviate shall be obtained from the acquiring activity.

5.2.6 Offset lands. Lands, when used in conjunction with clinched leads, may be located adjacent to (not surrounding) the lead termination hole. The land shall be a sufficient distance from the hole to allow clipping of the part lead prior to unsoldering the part lead from the land.

5.3 Holes.

5.3.1 Quantity. A separate component hole shall be provided for each lead or terminal of a part or end of wire jumper except as specified in 5.2 and 6.2.14.

5.3.2 Diameter of unsupported holes. The diameter of an unsupported terminal hole shall not exceed by more than 0.020 inch (0.51 mm) and shall be not less than 0.006 inch (0.15 mm) the nominal diameter of the lead to be inserted, unless it is clinched. The number of different hole sizes shall be kept to a minimum. When flat ribbon leads are mounted through unsupported holes, the difference between the nominal diagonal of the lead and the inside diameter of the unsupported hole shall not exceed 0.020 inch (0.51 mm) and shall be not less than 0.006 inch (0.15 mm), as shown on figure 15.

5.3.3. Eyelet hole diameter. Eyelets shall not be used in new design unless approved by the Government acquiring activity. When eyelets are used, the diameter of holes in which eyelets are inserted shall not exceed the outside diameter of the barrel of the eyelet by more than 0.006 inch (0.25 mm). The maximum inside diameter of the eyelets shall be not more than 0.028 inch (0.71 mm) greater or less than 0.006 inch than the nominal diameter of the lead or terminal to be inserted in the eyelet, unless the lead is clinched (see 6.1.2). Interconnections shall not be made with eyelets.

5.3.4. Spacing of adjacent holes. The spacing of unsupported or plated-through holes (or both) shall be such that the lands surrounding the holes meet the spacing requirements of 5.1.4. The spacing between adjacent holes of any other type shall be not less than the printed-wiring board thickness or the hole diameter, whichever is smaller.

5.3.5 Location. All land and hole locations shall be at the grid intersections of the modular dimensioning system (see 4.3) controlled by either primary or secondary grid systems (see 4.3.1) used for printed wiring except as specified in 5.3.5.1.

5.3.5.1 Pattern variations. Parts whose leads emanate in a pattern which varies from the grid intersections established by the master drawing shall be mounted or attached to the printed-wiring board with one of the following hole patterns:

a. A hole pattern where the hole for at least one part lead is located at a grid intersection of the modular dimensioning system and the other holes of the pattern are dimensioned from the grid location or from datum origin.
b. A hole pattern where the center of the pattern is located at a grid intersection of the modular dimensioning system and all holes of the pattern are dimensioned from that grid location or from datum origin.

5.3.6 Indexing holes. If indexing holes are to appear on the printed-wiring board, they shall be dimensioned on the master drawing.

5.4 Eyelets and standoff terminals. Eyelets and standoff terminals are to be considered components and specified on the assembly drawing.

5.4.1 Material. The eyelets shall be made of copper conforming to QQ-C-576. Standoff terminals shall be made of brass conforming to QQ-B-626 or bronze conforming to QQ-B-750.

5.4.2 Finish. The eyelets shall be tin-lead plated and fused (see 5.6.4.5). The standoff terminal shall be finished in accordance with 5.6.4.5 or 5.6.4.6 after having been underplated with 0.0001 inch (0.003 mm) minimum copper in accordance with MIL-C-14550.

5.4.3 Flange design. The flange used to make electrical contact to the terminal area shall be of the funnel flange type. The included angle of the flange shall be between 35 and 120 degrees. The rolled or flat flange shall be used when there will be contact with unclad material.

5.5 Plated-through holes. The maximum diameter of the plated-through hole shall not be more than 0.028 inch (0.71 mm) larger than the nominal of the inserted lead or the nominal diagonal of a flat ribbon lead, as shown on figure 15. The minimum diameter of the plated-through hole shall be not less than 0.006 inch (0.15 mm) larger than the nominal diameter of the inserted lead or nominal diagonal of a flat ribbon lead. Unless otherwise specified, the hole size shall be the finished plated size after solder coating or solder plating. Plated-through holes used for functional interfacial connections shall not be used for the mounting of devices which put the plated-through hole in compression. Plated-through holes used for functional interfacial connections shall not be used for the mounting of eyelets, standoff terminals, or rivets. The thickness of electrolytic copper plating in the hole shall be 0.001 inch (0.03 mm), minimum. The walls of plated-through holes shall be solder coated (see 5.6.4.6) or tin/lead plated and fused (see 5.6.4.5) as part of surface conductive cover requirements (see 5.6.4). Solder coating or tin-lead plating does not apply to plated-through holes which are internal to the printed-wiring board and do not extend to the surface. The end product diameter of plated-through holes shall be specified on the master drawing.

5.6 Materials. Printed-wiring board designs shall be such that internal temperature rise due to current flow in the conductor (see 5.1.1) when added to all other sources of heat at the conductor/laminate interface, will not result in an operating temperature in excess of that specified for the laminate material (see table IV). Since heat dissipated by parts mounted on the boards will contribute local heating effects, the material selection shall take this local factor, plus the equipments general internal rise in temperature, plus the specified operating ambient temperature for the equipment into account. Hot spot temperatures shall not exceed the temperatures specified in table IV for the laminate material selected. Materials used (copper-clad, prepreg, copper foil, heat sink, etc.) shall be specified on the master drawing.

5.6.1 Metal-Clad laminates. The printed-wiring boards shall be fabricated from the metal-clad laminates specified in table III and copper foil types specified in IPC-CF-150. The type of board(s) that each material may be used in is indicated in table IV.

TABLE IV. Clad laminates.

Specification	Base material	Operating temperature 1/	Board type 1	2	3
MIL-P-13949	PX	105°C	X	X	-
	GE, GF 2/	125°C	X 3/	X 3/	X
	GB, GH, GP, GT, GX, GR, GY	150°C	X	X	X
	GI 4/	170°C	X 3/	X 3/	X

1/ Ambient temperature plus the temperature rise caused by current in the conductors (see 5.1.1).
2/ GE or GF laminates shall not be combined in one board with GI prepregs.
3/ See 6.4.
4/ When GI laminates are combined in one board with GE or GF prepregs, the temperature shall be 125°C.

5.6.1.1 Minimum thickness of laminate. The thickness of the laminate per MIL-P-13949 used in type 3 printed-wiring boards shall be .002 inch (0.05 mm) or greater, provided the resulting dielectric layer in the finished board shall meet the requirements of 5.7.4. The thickness of the laminate per MIL-P-13949, used in type 1 and type 2 boards shall be as specified in the master drawing and shall meet the requirements of 6.4 (see figure 16).

5.6.2 Bonding materials.

5.6.2.1 Preimpregnated bonding layer (prepreg). Prepreg used in type 3 printed-wiring boards shall conform to type GE, GF, or GI of MIL-P-13949. Type GE or GF prepreg shall not be used with type GI prepreg. If a specific type of bonding material is required, it shall be so specified on the master drawing.

5.6.2.2 Other bonding films. Other bonding films such as cast resin films and double sided resin coated polyimide films may be used to bond external heat sinks, internal thermal planes, or internal conductive planes provided the cured films meet the temperature requirements of the base material as specified in table IV, 5.7.4, and on the master drawing.

5.6.3 Copper circuitry layers. The thickness of finished copper conductors shall be not less than 1 ounce per square foot (0.0012 inches). Copper foil used shall be not less than 1/2 oz/ft^2 and must be plated up to the 1 oz/ft requirement. (Precautionary note: A reduction of copper thickness after processing can be expected.)

5.6.4 Plating. All external conductive patterns (plated-through holes, terminal areas, etc.) shall be solder coated or tin-lead plated, unless a permanent solder mask coating is used (see 5.6.5) or a heat sink is bonded to the external surface, or other plating is approved by the acquiring activity. When other platings are used on the same printed-wiring board in conjunction with solder coating or tin-lead plating, the area of overlap shall be kept to a minimum and no exposed copper shall be permitted at the interface between the other plating and the solder coating or tin-lead plating. No solder or tin plating shall be under other platings. Unless otherwise specified on the master drawing, surface and plated-through hole plating thicknesses shall meet the requirements specified in 5.6.4.1 through 5.6.4.6.

5.6.4.1 Electroless copper plating. An electroless deposition system shall be used as a preliminary process for providing the conductive layer over nonconductive materials for subsequent electrodeposition of metal in plated-through holes.

5.6.4.2 Electrolytic copper plating. All electrolytically deposited copper plating shall be performed in accordance with MIL-C-14550, and shall have a minimum purity of 99.5 percent as determined by ASTM-E53. The minimum thickness shall be .001 inch (0.03 mm).

5.6.4.3 Gold plating. All electrolytically deposited gold shall be in accordance with MIL-G-45204, type II, class 1. The minimum thickness shall be 0.000050 inch (0.0013 mm); the maximum thickness shall be 0.0001 inch (0.003 mm) on areas that are to be soldered. A low stress nickel shall be used between gold overplating and copper (see 5.6.4.4).

5.6.4.4 Nickel plating. All electrolytically deposited nickel plating shall be low stress and conform to QQ-N-290, class 2, except the minimum thickness shall be .0002 inch (.005 mm).

5.6.4.5 Tin-lead plating. Tin-lead plating shall be in accordance with MIL-P-81728. The tin-lead shall be .0003 inch (.008 mm) thick minimum, as plated on the surface. Fusing shall be required on all tin-lead plated surfaces.

5.6.4.6 Solder coating. Unless otherwise specified, solder coating shall be in accordance with composition Sn60, Sn62, or Sn63 of QQ-S-571. The solder coating thickness shall be 0.0003 inch (0.008 mm) minimum, as coated (see 6.2.12 for surface mounted components).

5.6.5 Solder mask. Polymer mask coatings shall meet the requirements of IPC-SM-840, class 3 and, when required, shall be specified on the master drawing.

5.6.5.1 Solder mask over melting metals. Polymer mask coatings do not typically adhere to molten metals. When coatings are required over melting metal (such as solder) with areas of metal larger than 0.050 inch (1.3 mm) in two directions, the design shall provide relief through the metal to the printed-wiring substrate. The relief shall be at least 0.010 inch by 0.010 inch (0.25 mm by 0.25 mm) in size and located on a grid no greater than 0.250 inch (6.4 mm).

5.6.5.2 Solder mask over nonmelting metals. When polymer mask coatings are required over nonmelting metals (such as copper), the design shall provide that conductor areas not covered by the mask shall be tin/lead plated and fused (see 5.6.4.5) or solder coated (see 5.6.4.6). Bonding/adhesion promoters may be required (see 20.5).

5.7 Printed-wiring board dimensions. The board design shall meet the requirements specified in 5.7.1 through 5.7.5.

5.7.1 Overall board dimensions. Overall printed-wiring board dimensions (length and width), should coincide with lines of the modular dimensioning system.

5.7.2 Board thickness. The board thickness shall include metallic deposition, fusing, and solder mask, shall be measured across the board thickness extremities, and shall be as specified on the master drawing. In critical areas such as card guides, the thickness requirements shall be detailed on the master drawing.

5.7.3 Board thickness tolerance. The board thickness tolerance for types 1, 2, and 3 shall be as specified on the master drawing.

5.7.4 Minimum thickness of dielectric layers. Finished type 3 boards shall have a minimum of 0.0035 inch (.089 mm) of dielectric material between the consecutive conductor layers, when cured. Greater thicknesses should be considered for voltages greater than 100 volts. The dielectric material will be in accordance with MIL-P-13949 and may be comprised of laminate, prepreg and laminate, or multiple layers of prepreg. There shall be no less than two sheets of prepreg (B-stage) or laminate (C-stage), or combination thereof used between adjacent conductive layers. Other bonding films and thicknesses shall be specified on the master drawing (see 5.6.2.2 and figure 16).

NOTE: Thickness of dielectric layers shall be measured in accordance with MIL-P-55110.

5.7.5 Bow and twist. Unless otherwise specified on the master drawing, the maximum allowable bow and twist shall be 1.5 percent.

5.8 Detail board marking requirements. Individual printed-wiring boards and quality conformance test circuitry shall be identified in accordance with the master drawing and MIL-STD-130. Provision shall be made in the design for locating the traceability and date markings that are additionally required by the fabrication specification. The methods and materials for marking shall be specified on the master drawing. If ESD marking is required at the board level, it shall be specified on the master drawing. Marking shall be of a contrasting color to the background.

5.9 Quality conformance testing circuitry. The quality conformance test circuitry, comprised of the coupons shown on figure 1, shall be a part of every panel used to produce printed-wiring boards that are designed to this standard. The minimum number of coupons per panel and the requirements for positioning will be in accordance with table V. Coupons A, B, and F shall be positioned in accordance with 4.1 and figure 17. All other coupons may be positioned at optional locations. All coupons required shall be shown on the master drawing, artwork, and production master.

TABLE V. Conformance test circuitry.

Coupon type	Type 1 board	Type 2 board	Type 3 board
A Micro-section	Not required	Twice per panel opposite corners location fixed by artwork (see figure 17)	Twice per panel opposite corners location fixed by artwork (see figure 17)
B Micro-section	Twice per panel opposite corners location fixed by artwork (see figure 17)	Twice per panel opposite corners location fixed by artwork (see figure 17)	Twice per panel opposite corners location fixed by artwork (see figure 17)
C Plating	Once per panel location optional pattern defined by artwork	Once per panel location optional pattern defined by artwork	Once per panel location optional pattern defined by artwork
D Thermal shock	Not required	Once per panel location optional pattern defined by artwork	Once per panel location optional pattern defined by artwork
E 1/ Insulation resistance	Once per panel location optional pattern defined by artwork	Once per panel location optional pattern defined by artwork	Once per panel location optional pattern defined by artwork
F 2/ Registration	Not required	Not required	Twice per panel opposite corners location fixed by artwork (see figure 1)
J Solder mask	When required, once per panel with solder mask location optional pattern fixed by artwork	When required, once per panel with solder mask location optional pattern fixed by artwork	When required, once per panel with solder mask location optional pattern fixed by artwork

1/ If the panel has solder mask, the E coupon shall be covered with the solder mask. Clearances of 0.010 ±0.005 should be provided for all surface lands.
2/ Registration coupons are optional and may be used in lieu of microsection evaluation for registration.

6. DETAIL PART MOUNTING REQUIREMENTS

6.1 Approved methods of attachment. Component leads shall pass through lead component holes and be attached or the component terminals or leads shall be surface mounted to the land pattern. Part attachment shall be described on the assembly drawing following the methods specified in 6.1.2 through 6.1.5.4. General mounting requirements shall be as specified in 6.1.1.

6.1.1 Unclinched leads. Unless otherwise specified, unclinched leads (either straight or partially bent for retention) shall be soldered in component holes or eyelets in accordance with IPC-S-815. If no clinching requirements are specified on the assembly drawing, unclinched lead termination shall apply.

6.1.1.1 In unsupported holes. Lead tip projection shall be required to extend from 0.020 inch (0.51 mm) minimum to 0.060 inch (1.5 mm) maximum from the surface of the foil.

6.1.1.2 In plated-through or eyeletted holes. The lead shall be required to extend at least to the surface of the plating or rim of the eyelet and extend no more than 0.060 inch (1.5 mm) from the plating surface or eyelet.

6.1.2 Clinched leads. When maximum mechanical retention of a lead or terminal is required by design, the lead or terminal shall be clinched. The component holes may be plated-through holes, unsupported holes, or eyeletted holes. Clinching requirements shall be defined on the assembly drawing. The lead end shall not extend beyond the edge of its land or its electrically connected conductor pattern in violation of the minimum spacing requirement. Partial clinching of leads for part retention shall be considered under the requirements of 6.1.1.

6.1.3 Surface terminated ribbon leads. Flat-wire ribbon leads may be attached to lands on the printed-wiring board. Connections shall be made by soldering only. The contact area between any lead and land shall be not less than a square having each side equal to the nominal width of the lead (see figure 9). Minimum conductor spacing indicated in 5.1.4 shall be maintained. Attachment details may be conveyed by an assembly drawing reference to IPC-S-815 (see figure 18). For additional mounting notes and considerations see 6.2.11.

6.1.4 Surface terminated round leads. With prior approval by the government acquiring activity, designs may stipulate that parts shall be attached with their round leads soldered to surface terminals (lands) without first passing through a hole. The lands shall be designed with proper shape and spacing to comply with proper soldering techniques (see IPC-S-815).

6.1.5 Standoff terminals, eyelets, or fasteners.

6.1.5.1 Component attachment to standoffs. Component attachment to standoff terminals shall be defined on the assembly drawing and meet the requirements of IPC-S-815. *Placement of terminals shall be specified to suit each application.*

6.1.5.2 Attachment of standoffs to boards. A terminal of the funnel flanged type shall be specified wherever the flange must be soldered for electrical connection to a land. The included angle of such flange shall be between 35 and 120 degrees.

6.1.5.3 Eyelets. Eyelet applications used in design shall be in compliance with the following:

Attachment requirements - Interfacial connections shall not be made with eyelets. Eyelets installed at an electrically functional land shall be required to be of the funnel flange type.

6.1.5.4 Fastening hardware. The installed location and installation orientation shall be prescribed on the assembly drawing for any fastening devices such as rivets, machine screws, washers, inserts, nuts, and bracketing. Precautions such as the specification of tightening torque values shall be provided wherever general assembly practices might be inadequate or detrimental to the board assembly's structure or functioning.

6.2 Electrical part mounting. The following are requirements the designer shall consider and detail on the assembly drawing in specific notes or illustrations. All such electrical parts, hereafter referred to as components, shall also be selected so as to withstand the vibration, mechanical shock, humidity, and other environmental conditions the design must endure when the components are installed in accordance with 6.2.1 through 6.2.14.

6.2.1 One side only. Parts shall be mounted on only one side of the printed-wiring board assembly whenever possible.

6.2.2 Accessibility. Lands and terminals shall be located and spaced so that the terminations of each component are not obscured by any other component, or by any other permanently installed parts. Each component shall be capable of being removed from the assembly without having to remove any other component.

6.2.3 Design envelope. Unless otherwise detailed on the assembly drawing, the board edge is regarded as the extreme perimeter of the assembly, beyond which no portion of a component is allowed to extend. The designer shall prescribe the design envelope with due respect for maximum part body dimensions and the mounting provisions dictated by the board and assembly documentation.

6.2.4 Over conductive areas. No parts shall be mounted in direct contact with external conductor areas unless required for thermal dissipation. If design limitations require placement of parts over conductive areas, the part shall be mounted so that subsequent insulating coating will cover the conductive area under the part or conductive areas under parts shall be insulated or protected against moisture entrapment by applying conformal coating or a cured resin coating by laminating low-flow prepreg material in accordance with MIL-P-13949, or by solder masking over the area prior to mounting the part.

6.2.5 Thermal transfer. Components, which for thermal reasons require extensive surface contact with the board or with a heat sink mounted on the board, shall be protected from processing solutions at the conductive interface. To prevent risk of entrapment, compatible materials and methods shall be specified to seal the interface from entry of corrosive and conductive contaminants.

NOTE: Even totally nonmetallic interfaces that are prone to entrap fluids can have adverse effects on the fabricator's ability to pass required cleanliness tests.

6.2.6 Components dissipating one or more watts. Design for heat dissipation of components shall insure that the maximum allowable temperature of the board material is not exceeded under operating conditions specified in 5.6. Heat dissipation may be accomplished by requiring a gap between board and component, using a clamp or thermal mounting plate, or attaching a compatible, thermally conductive material working in conjunction with a thermal bus plane to the component.

6.2.7 Stress relief bends. Lands and terminals shall be located by design so that components can be mounted or provided with stress relief bends in such a manner that the leads cannot overstress the part lead interface when subjected to the anticipated environments of temperature, vibration, and shock of MIL-P-28809. The lead length for stress relief and lead bend radius shall be in accordance with figure 19. Where lead bending can not be in accordance with figure 19 in order to achieve design goals, the bends shall be detailed on the assembly drawing.

6.2.8 Mechanical support. All parts weighing 0.25 ounce (7.1g) or more per lead shall be supported by clamps or other specified means which will insure that the soldered joints and leads are not relied upon for mechanical strength.

6.2.9 Axial-leaded parts. Axial-leaded parts shall be mounted as specified on the approved assembly drawing and mounted so that a portion of the body is as close to the printed-wiring board as possible. The leads shall be shaped in accordance with 6.2.7. This does not apply to parts mounted on standoff terminals (see 6.1.5.1).

6.2.9.1 Perpendicular mounting. Axial-leaded components weighing less than 0.50 ounce (14g) may be mounted on the assembly using perpendicular mounting criteria. The assembly drawing shall prescribe a minimum of 0.015 inch (0.38 mm) space between the end of the component body (or the lead-weld) and the board. Unless otherwise noted on the assembly drawing, components required to be perpendicularly mounted shall be installed with their major axis within ±15 degrees of a right angle with board surface. The maximum vertical height from the board surface shall be 0.55 inch (14 mm) (see figure 20).

6.2.10 Nonaxial-leaded parts. Nonaxial-leaded parts shall be mounted with the surface from which the lead projects a minimum of 0.010 inch (0.25 mm) above the printed-wiring board surface. Dimensioning of the required spacing under these components is generally not required unless the component package design could result in an assembly error. For thermal considerations see 6.2.5 and 6.2.6.

6.2.11 Multiple-leaded components. Multiple-leaded components (components with three or more leads), except multiple leaded components mounted to thermal planes or heat sinks, shall be mounted in such a manner that components are spaced off the board to facilitate cleaning, provide electrical isolation, and to prevent moisture traps. The necessary gap may be prescribed as an exceptional fabrication requirement by identifying the subject component and prescribing the required underbody clearance dimension or the gap may be achieved by virtue of the component's own standoff features. Unless otherwise specified, a clearance of 0.010 inch (0.25 mm) minimum applies.

6.2.11.1 Spacers. Special spacers (such as feet, ribs, or projections) with minimal contact may be prescribed to go under the component, provided they will not impair soldering or the assembly's performance.

6.2.11.2 Sealing. The need for a gap between component body and board may be avoided by requiring the interface under the component to be sealed with adhesive or a combination of adhesive and insulation material, which is compatible with the board, parts, and conformal coating. This option exists only if all lead terminations are external to the seal. Repairability shall not be precluded by the method or material selection.

6.2.12 Surface mounted components. The requirements and considerations of 6.2.4 apply to this class of components. Space for cleaning shall be provided to reduce entrapment.

6.2.12.1 Flat-pack types with ribbon leads. Lead forming is a major design consideration and shall be detailed on the assembly drawing to provide for lead stress relief, fit to the land pattern, underbody clearance for cleaning, and any designed-in provisions for thermal transfer (see figure 18 and 6.1.3).

6.2.12.2 Chip carrier type. Leadless components may be attached to the surface of a land. The component shall be attached to the land of the printed-wiring board in a way that provides sufficient space under the body of the component to facilitate cleaning. Land pattern design shall facilitate adequate solder fillets between the conductor pattern and the component.

6.2.12.3 End-cap discrete components. End-cap discrete resistor and capacitor components and similar leadless end-cap discrete components shall be mounted to printed wiring or printed circuitry. The devices shall not be stacked nor shall they bridge spacing between other parts or components, such as terminals or other properly-mounted components.

6.2.12.4 Surface mounting of flattened round leaded components. Components with axial leads of round cross-sections shall be utilized for surface mounting only if the leads are coined or flattened for positive receding. For flattened round leads with original diameter of 0.025 inch (0.635 mm) or greater, the flattened thickness shall be 70 percent of the original diameter, minimum. For leads with an original diameter less than the 0.025 inch (0.635 mm), the flattened thickness shall be 50 percent of the original diameter, minimum. The body of a planar mounted axial leaded component should be spaced away from the board to facilitate cleaning.

6.2.13 Two-part connectors (plug and receptacle). Two-part connectors containing male and female quick disconnect electrical contacts and integral aligning hardware to assure proper mating of the contacts shall be specified as the only means to integrate plug-in printed-wiring assemblies. Their attachment and mounting methods are subject to the design concerns of 6.1, 6.2.3, and 6.2.4. Board connectors may be uniquely keyed in such a manner only insertion of the proper assembly is possible.

6.2.13.1 Wires. Use of hard wiring directly to plug in connector mounted printed-wiring board assemblies shall not be permitted. Plug in assemblies shall have all external electrical connections accomplished through the use of two-part connectors.

6.2.14 Jumper wires. Jumper wires may be used on types 1, 2, or 3 printed-wiring board assemblies. Jumper wires shall be terminated in holes or standoffs. They may also be terminated on lands with prior approval of the government acquiring activity. Jumper wires shall be considered a component. Jumper wires shall be as short as practicable and shall not be applied over or under other replaceable components (including jumper wires). Jumper wires must be permanently fixed to the printed-wiring board at intervals not to exceed 1 inch. Jumper wires less than 0.50 inch in length whose path does not pass over conductive areas and does not violate the spacing requirements (see 5.1.4) may be uninsulated. Insulation, when required, or jumper wires shall be compatible with the conformal coating.

6.3 Conformal coating. The design criteria contained in this standard are predicated on the requirement that end item assemblies shall be conformally coated. Solder mask shall not be used in lieu of conformal coating.

6.3.1 Coating area. Printed-wiring assemblies shall be conformally coated with a coating material that conforms to MIL-I-46058. The coating shall be applied to both sides of the cleaned printed-wiring assembly including the part leads. The type of conformal coating shall be listed on the assembly drawing.

6.3.1.1 Surfaces to be free of coating. Surfaces specified on the approved assembly drawing to be free of conformal coating shall be suitably masked and protected from coating, coating residues, and masking residues. The masking material used shall have no deleterious effects on the printed-wiring boards. Printed-wiring assemblies having adjustable components shall not have the adjustable portion covered with coating. Electrical and mechanical mating surfaces, such as probe points, screw threads, bearing surfaces, and so forth shall not be coated.

6.3.2 Cleaning agents. Cleaning agents and techniques shall have no deleterious effects on any part of the printed-wiring assembly.

6.3.3 Compatibility. The conformal coating shall be compatible with all parts of the printed-wiring assembly.

6.3.4 Thickness. The thickness of the conformal coating shall be as follows for the type specified, when measured on a flat unencumbered surface:

a. Types ER, UR, and AR: 0.003 ±0.002 inch (0.08 ±0.05 mm).
b. Type SR: 0.005 ±0.003 inch (0.13 ±0.08 mm).
c. Type XY: 0.0005 to 0.002 inch (0.010 to 0.05 mm).

6.3.5 Electrical performance. Printed-wiring assemblies shall be constructed, adequately masked, or otherwise protected in such a manner that application of conformal coating does not degrade the electrical performance of the assembly.

6.3.6 Buffer material. If component(s) on the printed-wiring assembly are made of brittle material (glass or ceramic), they shall be protected against breakage by a buffer material before applying the conformal coating to the assembly. The buffer material shall be a thin, pliant material such as polyvinylidene fluoride, polyethylene terephthalate, or silicon rubber, and be nonreactive with the conformal coating material and all parts of the printed-wiring assembly. The buffer material shall be fungus resistant and flame retardant, and clear or transparent, so markings on the components are visible.

6.3.6.1 When required. When conformal coating types SR, XY, UR, and AR are used, buffer material is not required. Buffer material will be required for type ER.

NOTE: Board designers are cautioned to consider that buffer material may be needed when allocating space and location for components to be mounted on printed-wiring boards covered by this standard.

6.4 Support. All printed-wiring assemblies shall be supported within a maximum of 1 inch (25.4 mm) of the edges on at least two opposite sides. Support shall be sufficient to prevent fracture or loosening of the foil or breakage of the parts or part leads resulting from flexing of the printed-wiring boards.

6.5 Detailed assembly markings. Completed printed wiring assemblies shall be marked in accordance with the assembly drawing and MIL-STD-130 with their full identification. Printed-wiring assemblies which contain electrostatic discharge sensitive devices shall be marked in accordance with DOD-STD-1686. The marking shall be etched or applied by the use of a permanent ink which will withstand assembly processing. Additional markings if required shall be specified on the assembly drawing.

APPENDIX

10. SCOPE

10.1 Purpose. This appendix is for guidance to the designer of printed-wiring boards.

20. DESIGN CONSIDERATIONS

20.1 Design process tolerances and allowances. The data in table VI shall serve as a guide concerning the tolerances and allowances used in the design process. Due to tolerance buildup, the tradeoffs involved in arriving at the permissible limits for each particular tolerance for a particular design should be recognized. This data is intended to show the increasing difficulty of producing boards with tighter tolerances, but does not express the limits attainable or permissible for any single aspect of board design. This data shall not be interpreted as end item board requirements.

20.2 Board dimensions. Extreme length-to-width ratios should be avoided.

20.3 Dimensional stability. While MIL-P-13949 limits the allowable dimensional change of the thin laminate, consideration must be given to the fact that during processing, the thin laminate may either expand or contract within these limits, and in addition, the change may vary across different portions of the board. The result may be misregistration, and bow and twist beyond that which would be expected from a simple dimensional change.

20.4 Dielectric constant and dissipation factor. When designing circuits which depend on stable dielectric properties, consideration should be given to the fact that MIL-P-13949 sets forth only a maximum for these values and that some materials which meet the thin laminate specifications will have values 15 percent lower than the specification requirement.

20.5 Surface preparation of large conductive areas. The adhesion of prepregs and other polymers, such as solder mask to large conductive areas, may be improved through the use of special materials and surface preparations. The use of adhesion promoters, such as oxide treatments and double treated copper may improve the bonding of type 3 printed-wiring boards. A protective chemical treatment may be required to prevent a reaction between the copper surface and the polymer coating.

20.6 High voltage factors (considerations):

a. Encapsulate with void-free potting materials, well bonded to all surfaces.
b. Avoid sharp projections.
c. Arrange conductors so that high and low voltage groups are separate from one another.
d. Provide rounded corners on electrical conductors and ground planes next to energized circuits.
e. In ac circuits, check adjacent conductors for instantaneous voltage differences between them.
f. Conformal coating should consist of at least three separate layers, with each layer applied at right angles to the previous layer.
g. Solder terminations on the printed-wiring board must be smooth and even with no projections from the component lead or solder spikes.
h. Standoff terminal connections must be solder balled. The radius of the solder ball should be at least 1/6 of the spacing between the solder ball and adjacent high voltage circuit or ground plane. When large spacings are involved, the solder ball should be at least .125 inch (3.1 mm) in diameter.

TABLE VI. Composite board design guidance.

	Preferred	Standard	Reduced producibility
Number of conductor layers (maximum 1/)	6	12	20
Thickness of total board (maximum) (inch)	0.100(2.54)	0.150(3.81)	0.200(5.08)
Board thickness tolerance	±10% of above nominal or 0.007(0.18), whichever is greater		
Thickness of dielectric (minimum)	0.008(0.20)	0.006(0.15)	0.004(0.10)
Minimum conductor width (or figure 4 value, whichever is greater)			
Internal	0.015(0.38)	0.010(0.25)	0.004(0.10)
External	0.020(0.51)	0.015(0.38)	0.004(0.10)
Conductor width tolerance			
Unplated 2 oz/ft^2	+0.004(0.10) -0.006(0.15)	+0.002(0.05) -0.005(0.13)	+0.001(0.025) -0.003(0.08)
Unplated 1 oz/ft^2	+0.002(0.05) -0.003(0.08)	+0.001(0.025) -0.002(0.05)	+0.001(0.025) -0.001(0.025)
Protective plated (metallic etch resist over 2 oz/ft^2 copper)	+0.008(0.20) -0.006(0.15)	+0.004(0.10) -0.004(0.10)	+0.002(0.05) -0.002(0.05)
Minimum conductor spacing (or table I, whichever is greater)	0.020(0.51)	0.010(025)	0.005(0.13)
Annular ring plated-through hole (minimum)			
Internal	0.008(0.20)	0.005(0.13)	0.002(0.05)
External	0.010(0.25)	0.008(0.20)	0.005(0.13) 2/
Feature location tolerance (master pattern, material movement, and registration (rtp)			
Longest board dimension 12" or less	0.008(0.20)	0.007(0.18)	0.006(0.15)
Longest board dimension over 12"	0.010(0.25)	0.009(0.23)	0.008(0.20)
Master pattern accuracy (rtp)			
Longest board dimension 12" or less	0.004(0.10)	0.003(0.08)	0.002(0.05)
Longest board dimension over 12"	0.005(0.13)	0.004(0.10)	0.003(0.08)
Feature size tolerance	±0.003(0.08)	±0.002(0.05)	±0.001(0.025)
Board thickness to plated hole diameter (maximum)	3:1	4:1	5:1
Hole location tolerance (rtp)			
Longest board dimension 12" or less	0.005(0.13)	0.003(0.08)	0.002(0.05) 3/
Longest board dimension over 12"	0.007(0.18)	0.005(0.13)	0.003(0.08) 3/
Unplated hole diameter tolerance (unilateral)			
Up to 0.032(0.81)	0.004(0.10)	0.003(0.08)	0.002(0.05)
0.033(0.84)-0.063(1.61)	0.006(0.15)	0.004(0.10)	0.002(0.05)
0.064(1.63)-0.188(4.77)	0.008(0.20)	0.006(0.15)	0.004(0.10)

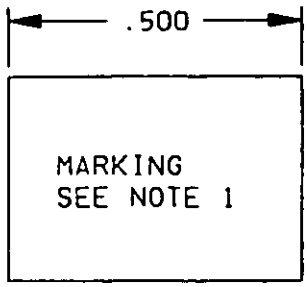
See footnotes at the end of table.

TABLE VI. Composite board design guidance - Continued.

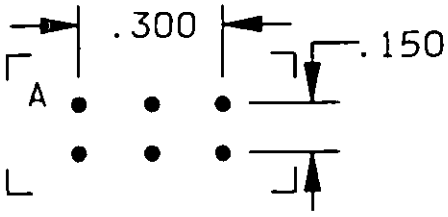
	Preferred	Standard	Reduced Producibility
Plated hole diameter tolerance (unilateral) for minimum hole diameter maximum board thickness ratios greater than 1:4 add 0.004(0.01)			
0.015(0.38)-0.030(0.76)	0.008(0.20)	0.005(0.13)	0.004(0.10)
0.031(0.79)-0.061(1.56)	0.010(0.25)	0.006(0.15)	0.004(0.10)
0.062(1.59)-0.186(4.75)	0.012(0.31)	0.008(0.20)	0.006(0.15)
Conductor to edge of board (minimum)			
Internal layer----------	0.100(2.54)	0.050(1.27)	0.025(0.64)
External layer----------	0.100(2.54)	0.100(2.54)	0.100(2.54)

1/ The number of conductor layers should be the optimum for the required board function and good producibility.
2/ See 5.2.3.
3/ To be used only in extreme situations warranted by the application.

NOTE: Unless otherwise specified, all dimensions and tolerances are in inches; data in parentheses () is expressed in millimeters.

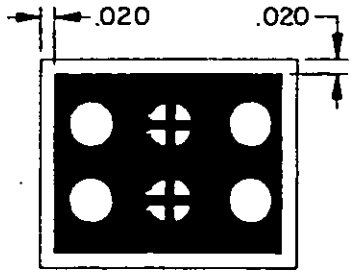


COUPON "A"



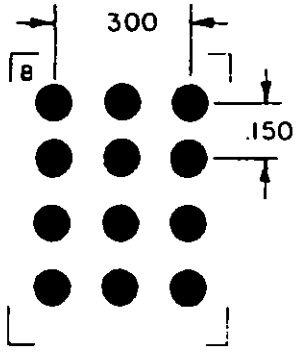
TYPICAL OF SURFACE LAYERS AND INTERNAL CIRCUIT LAYERS

See note 10 and 12



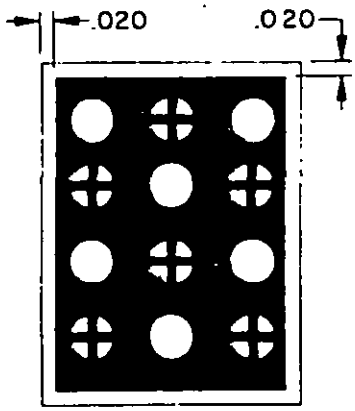
TYPICAL OF INTERNAL PLANE LAYERS

COUPON "B"



TYPICAL OF SURFACE LAYERS AND INTERNAL CIRCUIT LAYERS

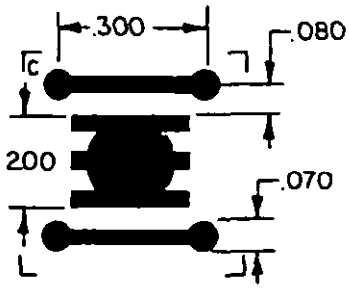
See note 12



TYPICAL OF INTERNAL PLANE LAYERS

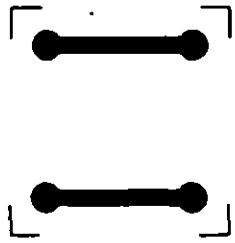
FIGURE 1. Quality conformance test circuitry.

COUPON "C"

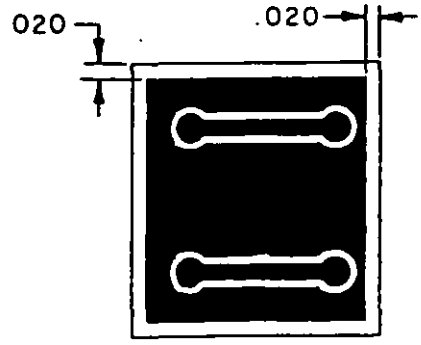


TYPICAL OF
SURFACE
LAYERS
TYPE 1, 2, 3
BOARDS

See Note 12

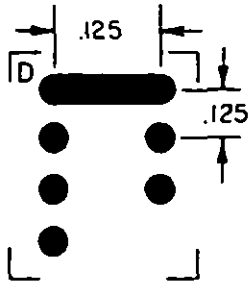


TYPICAL OF
INTERNAL
CIRCUIT
LAYERS
TYPE 3
BOARDS

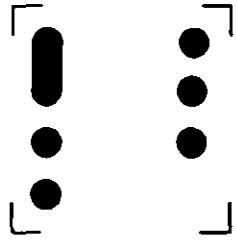


TYPICAL OF
INTERNAL
PLANE
LAYERS
TYPE 3
BOARDS

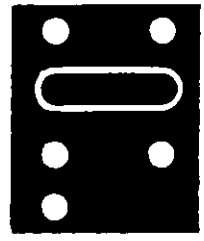
COUPON "D"



LAYER 1
TYPE 2 AND 3
BOARDS



LAYER 2
TYPE 2 AND 3
BOARDS TYPICAL
OF INTERNAL
CIRCUIT LAYERS

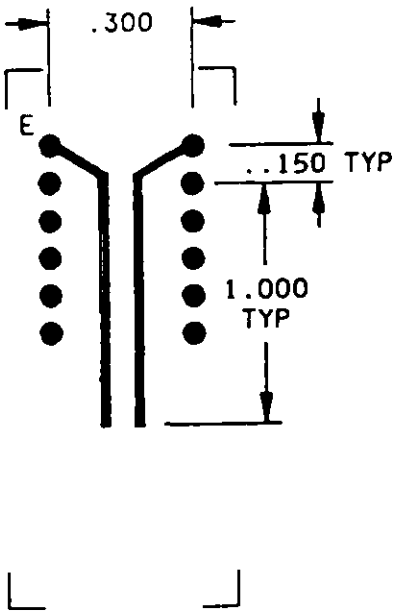


TYPICAL OF
INTERNAL
PLANE LAYERS
TYPE 3 BOARDS

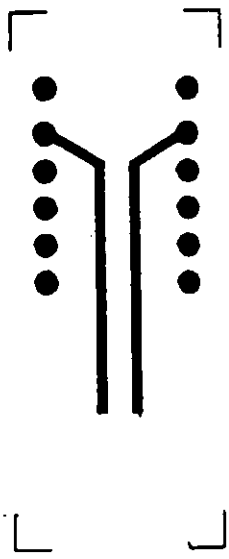
See notes 8, 9, and 12.

FIGURE 1. Quality conformance test circuitry - Continued.

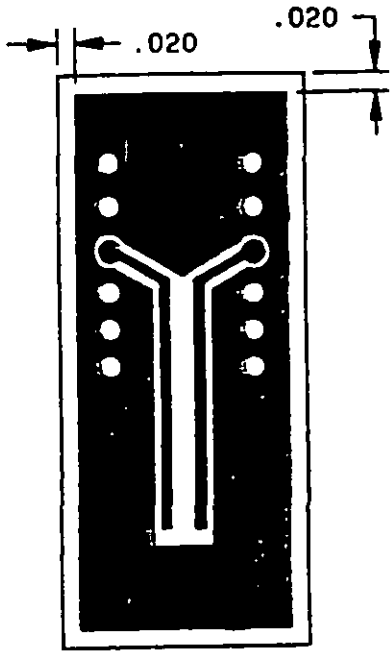
COUPON "E"



LAYER 1 OF
TYPE 1, 2,
AND 3 BOARDS



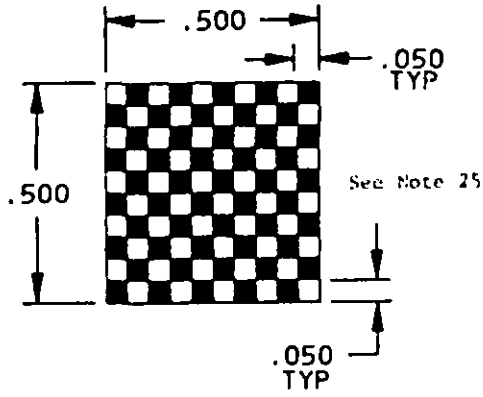
LAYER 2 OF
TYPE 2 AND
3 BOARDS
TYPICAL OF
INTERNAL
CIRCUIT
LAYERS



TYPICAL OF
INTERNAL
PLANES OF
TYPE 3
BOARDS

See Notes 8, 11, and 12.

COUPON "J"

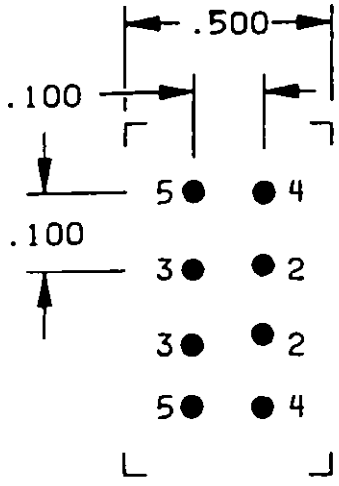


SURFACE
LAYERS ONLY
TYPE 1, 2
AND 3 BOARDS

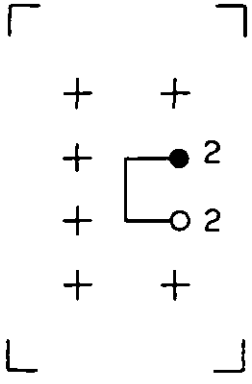
See Notes 12 and 16.

FIGURE 1. Quality conformance test circuitry - Continued.

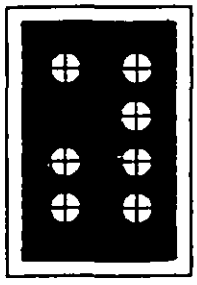
COUPON "F"



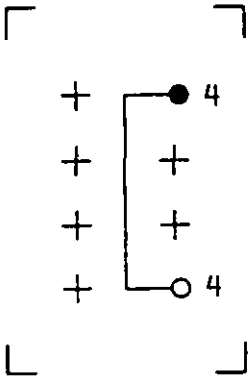
(a.)
SURFACE LAYERS,
TYPICAL



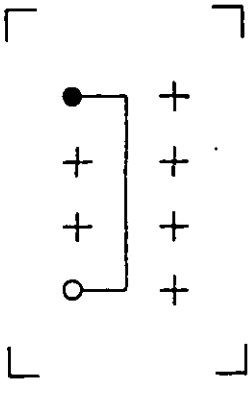
(b.)
LAYER 2
INTERNAL



(c.)
LAYER 3
TYPICAL OF
INTERNAL
PLANE LAYER



(d.)
LAYER 4
INTERNAL



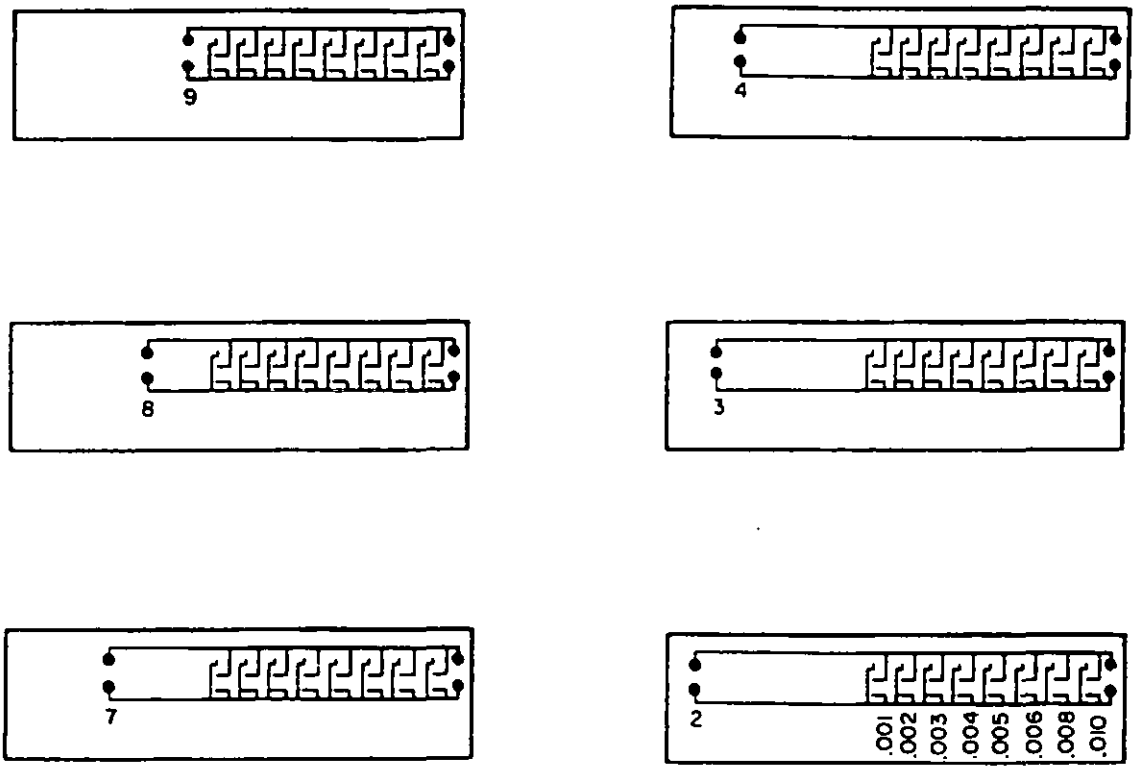
(e.)
LAYER 5
INTERNAL

Layer-to-layer registration (optional design).

See notes 18 thru 24

FIGURE 1. Quality conformance test circuitry - Continued.

Coupon F, layer-to-layer registration (optional design).

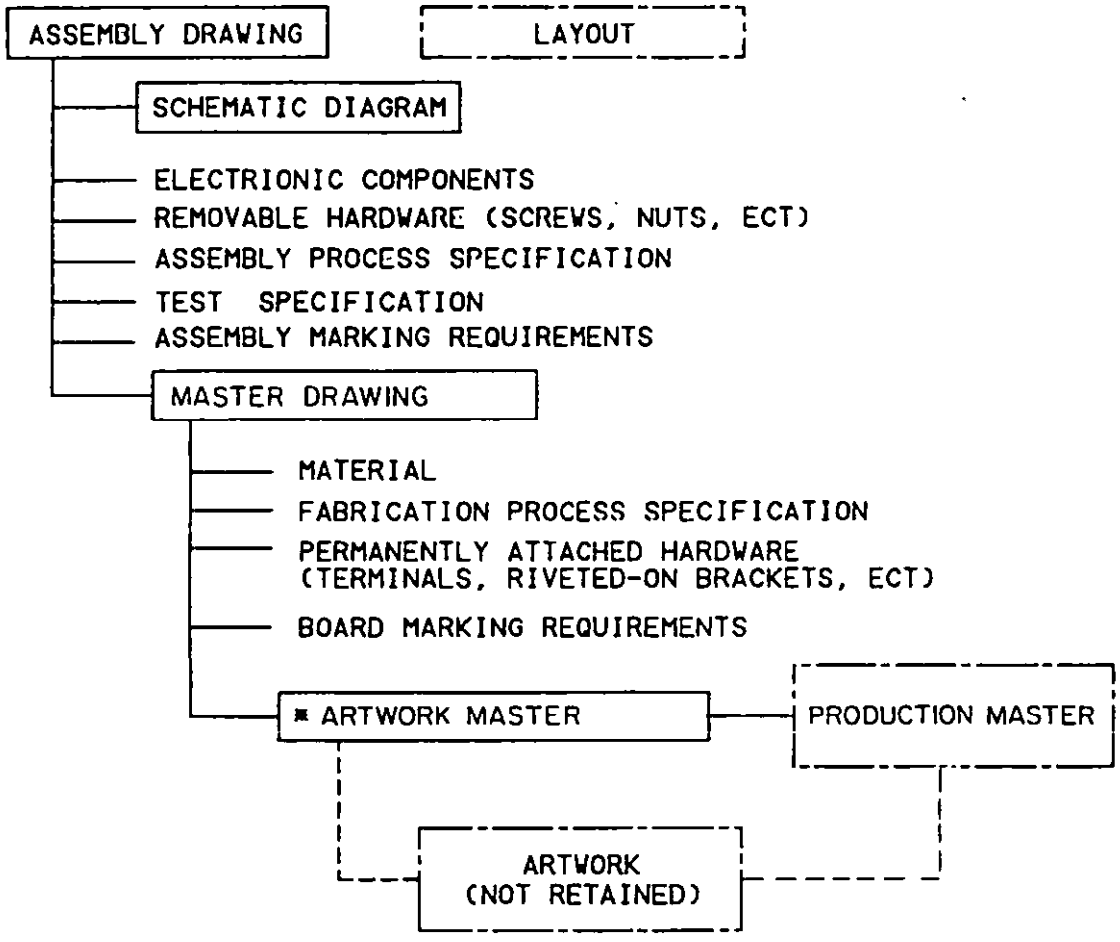


See notes 18 thru 24.

FIGURE 1. Quality conformance test circuitry - Continued.

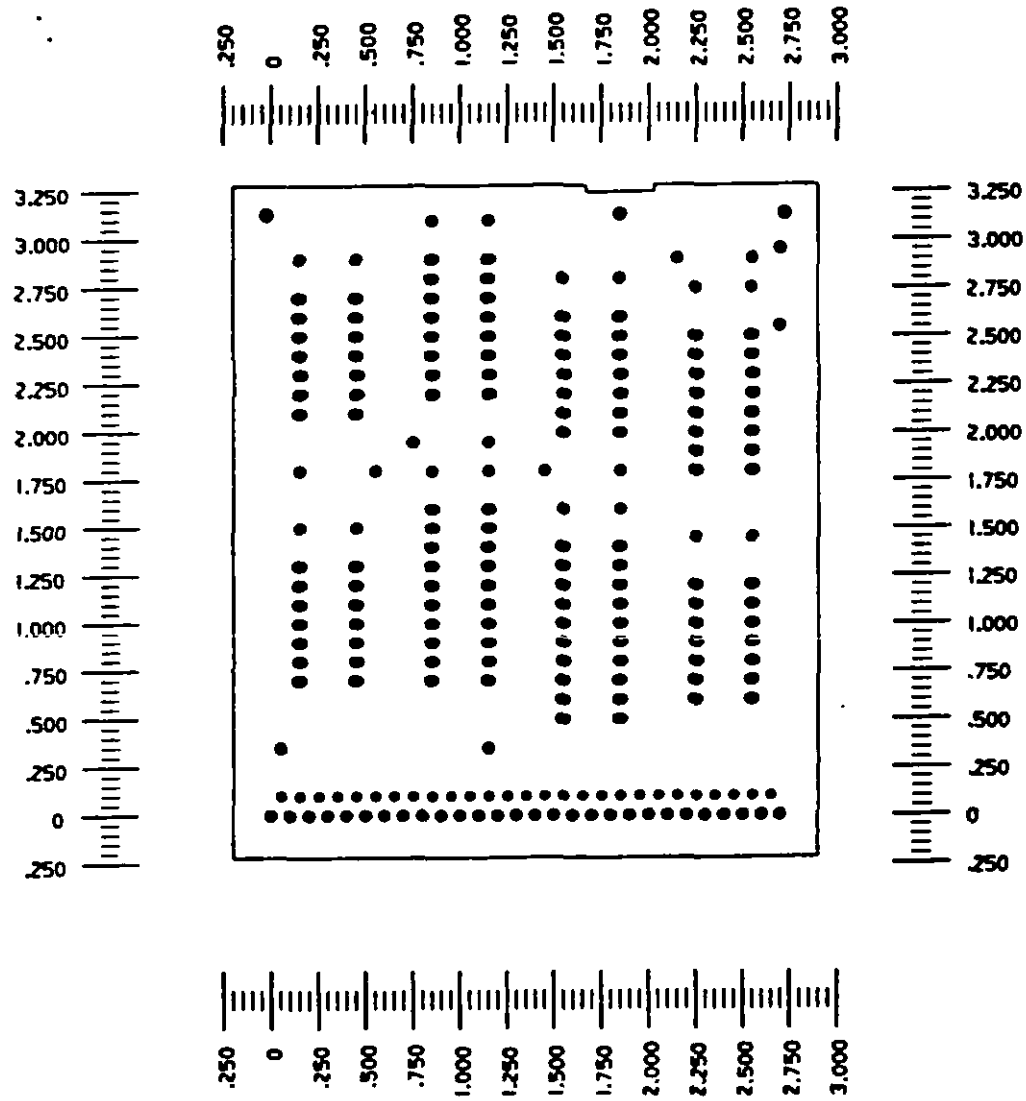
NOTES:
1. Test coupons are to be identified with the following:
   a. FSCM of board manufacturers.
   b. Part number and revision letter of master drawing.
   c. Board traceability and lot number.
2. Dimensions are in inches.
3. Metric equivalents are given for general information only.
4. Unless otherwise specified, all conductors shall be .020 inch (0.51 mm) ±.003 (0.08 mm) wide.
5. Unless otherwise specified, the tolerances shall meet the requirements of this specification.
6. Unless otherwise specified, the minimum land dimension shall be .070 inch (1.78 mm) ±.005 inch (0.13 mm) and may represent the land shape used on the associated board. Holes in the land areas shall be the diameter of the smallest component hole in the associated board (see note 10).
7. Coupons for surface layers or internal layers shall be representative of the type of circuitry on the associated layer. Any layer with large copper planes shall use the appropriate plane coupon where applicable on the layer that is being represented by the coupon.
8. The lengths of coupons D, E, and F are dependent upon the number of layers in the panel.
9. For coupon D, a pair of holes and a conductor between same shall be provided for each layer. Electrical connection shall be in series, stepwise, through each conductor layer of the board.
10. For coupons A and B, the minimum land dimension and shape shall be that used on the associated board. The hole shall be the maximum used in this minimum land dimension.
11. For coupon E, a pair of holes, and the conductor width and spacing shall be .025 ±.005 inch.
12. The quality conformance test circuitry may be segmented; however, coupons A, B, and F, when required, must be joined together. Coupons C, D, E, and J may be arranged to optimize board layout. All test coupons illustrated when required must appear on each panel. The number of layers must be identical to the associated board.
13. Etched letters on coupons are for identification purposes only.
14. The number of layers shown in these test coupons are for illustration purposes only. Conductor layer number 1 shall be the first layer on the component side, and all other conductor layers shall be counted consecutively downward through the laminated board to the bottom conductor layer which is the solder side.
15. For coupon F, the design is optional, provided the coupon defines the relationship of the features on each conductor layer to the board datum. For examples of coupons used for registration evaluation of type 3 boards.
16. Coupon J is only required on board surfaces to be solder mask coated.
17. Spacing between coupons may be modified to accommodate tooling holes used for automatic and/or multiple mounting microsectioning equipment.
18. The land dimension should represent the smallest land used for a component hole in the associated board.
19. The holes in the lands should be the diameter of the smallest components in the associated board.
20. The inside diameter of the circular lands should be design dimension minus 2 x .002 inch. (Additional allowances may be made for the etch allowance used in the associated board.)
21. The clearance hole in the planes used for the specific layer evaluation should be design dimension minus 2 x .002 inch. All other clearances should be a minimum of design dimension plus 2 x .002 inch. (Additional allowances may be made for the etch allowances used in the associated board.)
22. The conductor dimensions should be representative of the associated board.
23. The coupon may be reduced or extended to accommodate the number of layers in a type 3 board.
24. If continuity exists between commonly number lands, the board does not meet the minimum annular ring requirement of 0.002 inch.
25. Dark squares represent metal.

FIGURE 1. Quality conformance test circuitry - Continued.



* Includes circuit and silk screen masters.

FIGURE 2. Block diagram depicting typical printed-wiring drawing relationships.



NOTE: Scales may be located as shown or at the edge of the artwork.

FIGURE 3. Use of grids in defining pattern requirements.

(For use in determining current carrying capacity and sizes of etched copper conductors for various temperature rises above ambient)

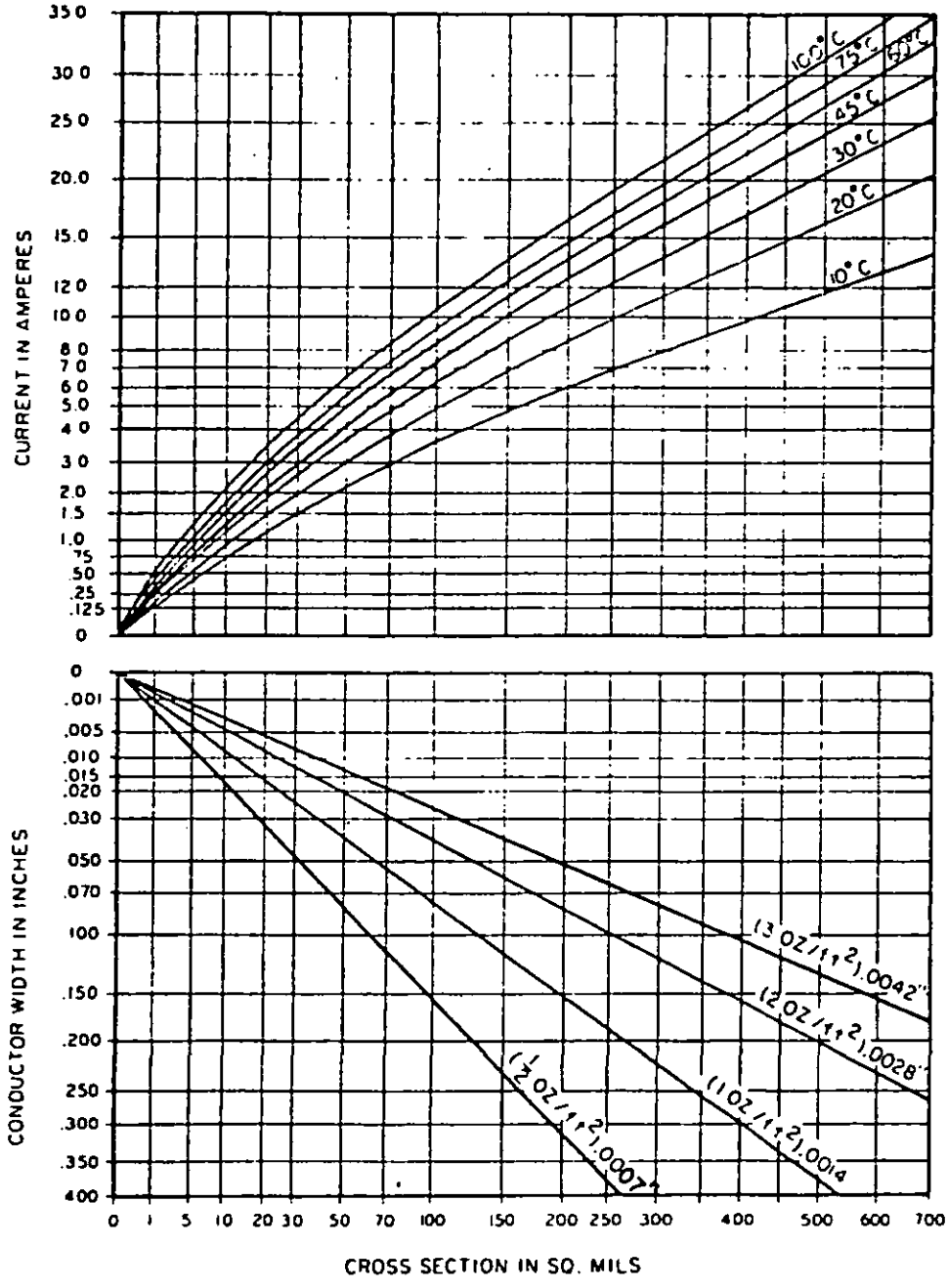


FIGURE 4a. Conductor thickness and width for type 1, type 2, and external layers of type 3 printed-wiring boards.

NOTES:

1. The design chart has been prepared as an aid in estimating temperature rises (above ambient) vs current for various cross sectional areas of etched copper conductors. It is assumed that for normal design conditions prevail where the conductor surface area is relatively small compared to the adjacent free panel area. The curves as presented include a nominal 10 percent derating (on a current basis) to allow for normal variations in etching techniques, copper thickness, conductor width estimates, and cross-sectional area.
2. Additional derating of 15 percent (current-wise) is suggested under the following conditions:
   (a) For panel thickness of 1/32 inch or less.
   (b) For conductor thickness of 0.0042 inch (3 oz/ft^2) or thicker.
3. For general use the permissible temperature rise is defined as the difference between the maximum safe operating temperature of the laminate and the maximum ambient temperature in the location where the panel will be used.
4. For single conductor applications, the chart may be used directly for determining conductor widths, conductor thickness, cross-sectional area, and current-carrying capacity for various temperature rises.
5. For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross-section and an equivalent current. The equivalent cross-section is equal to the sum of the cross-sections of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.
6. The effect of heating due to attachment of power dissipating parts is not included.
7. The final conductor thickness in the design chart do not include conductor overplating with metals other than copper.

FIGURE 4a. Conductor thickness and width for type 1, type 2, and external layers of type 3 printed-wiring boards - Continued.

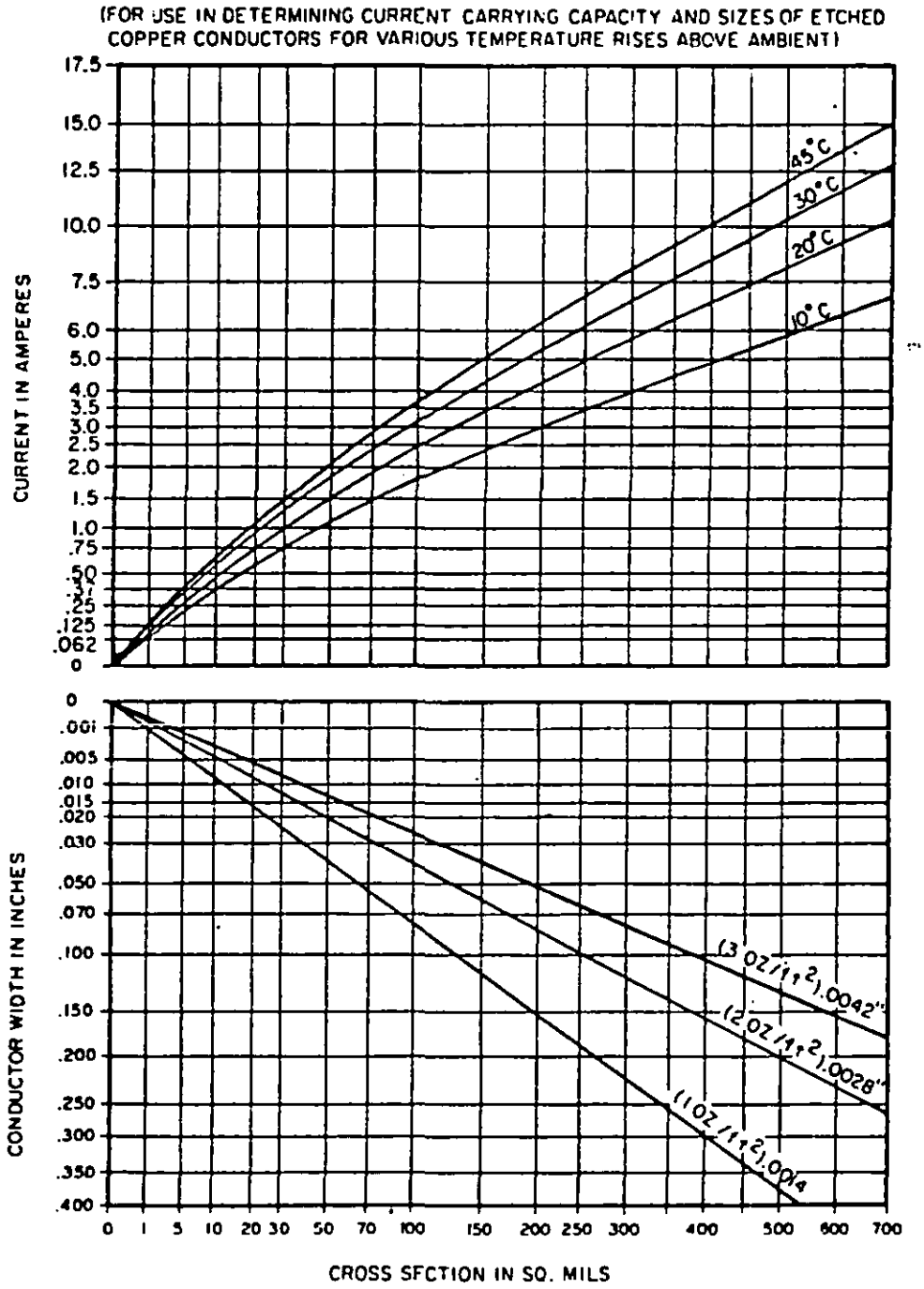


FIGURE 4b. Conductor thickness and width for internal layers of type 3 boards.

NOTES:

1. The design chart has been prepared as an aid in estimating temperature rises (above ambient) vs current for various cross-sectional areas of etched copper conductors. It is assumed that for normal design conditions prevail where the conductor surface area is relatively small compared to the adjacent free panel area. The curves as presented include a nominal 10 percent derating (on a current basis) to allow for normal variations in etching techniques, copper thickness, conductor width estimates, and cross-sectional area.
2. Additional derating of 15 percent (current-wise) is suggested under the following conditions:
   (a) For panel thickness of 1/32 inch or less.
   (b) For conductor thickness of 0.0042 inch (3 oz/ft^2) or thicker.
3. For general use the permissible temperature rise is defined as the difference between the maximum safe operating temperature of the laminate and the maximum ambient temperature in the location where the panel will be used.
4. For single conductor applications, the chart may be used directly for determining conductor widths, conductor thickness, cross-sectional area, and current-carrying capacity for various temperature rises.
5. For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross-section and an equivalent current. The equivalent cross-section is equal to the sum of the cross-sections of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.
6. The effect of heating due to attachment of power dissipating parts is not included.
7. The final conductor thickness in the design chart do not include conductor overplating with metals other than copper.
8. The current may be up-rated 100 percent for external circuitry.

FIGURE 4b. Conductor thickness and width for internal layers of type 3 boards - Continued.

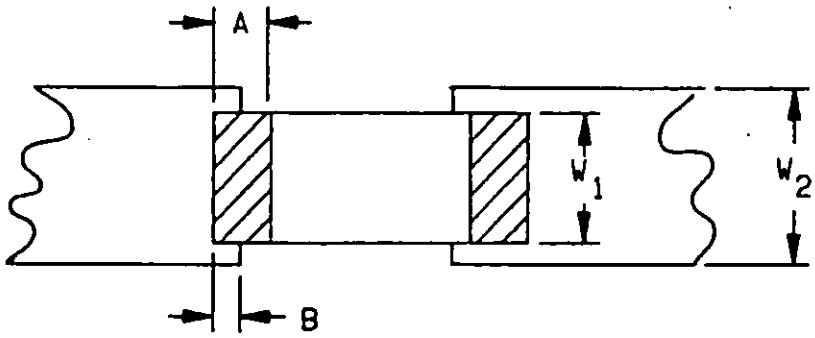


FIGURE 5. Discrete leadless component land pattern.

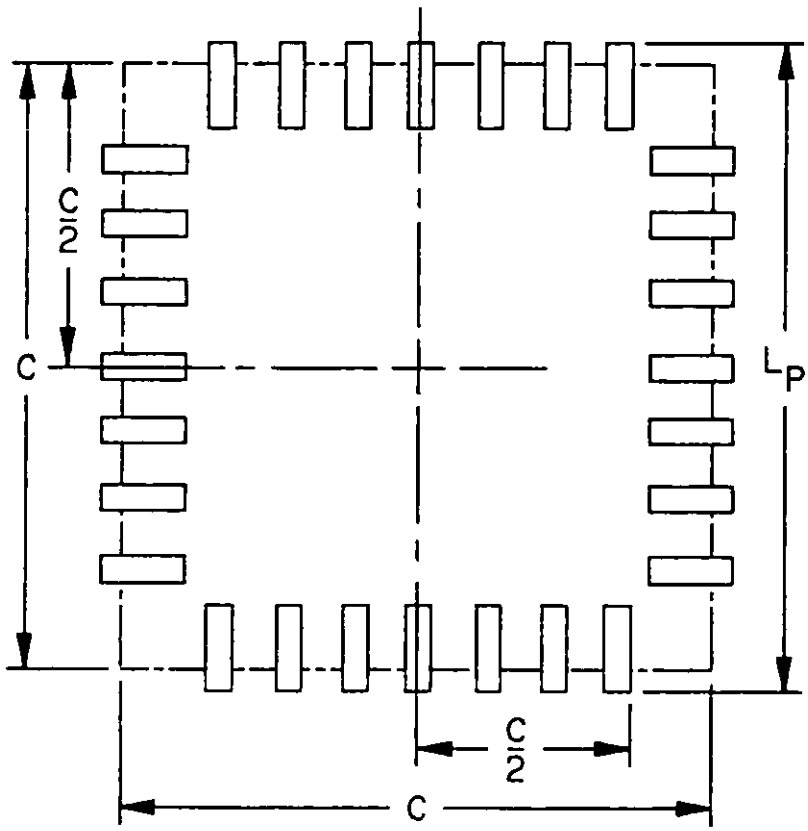


FIGURE 6. Chip carrier land pattern.

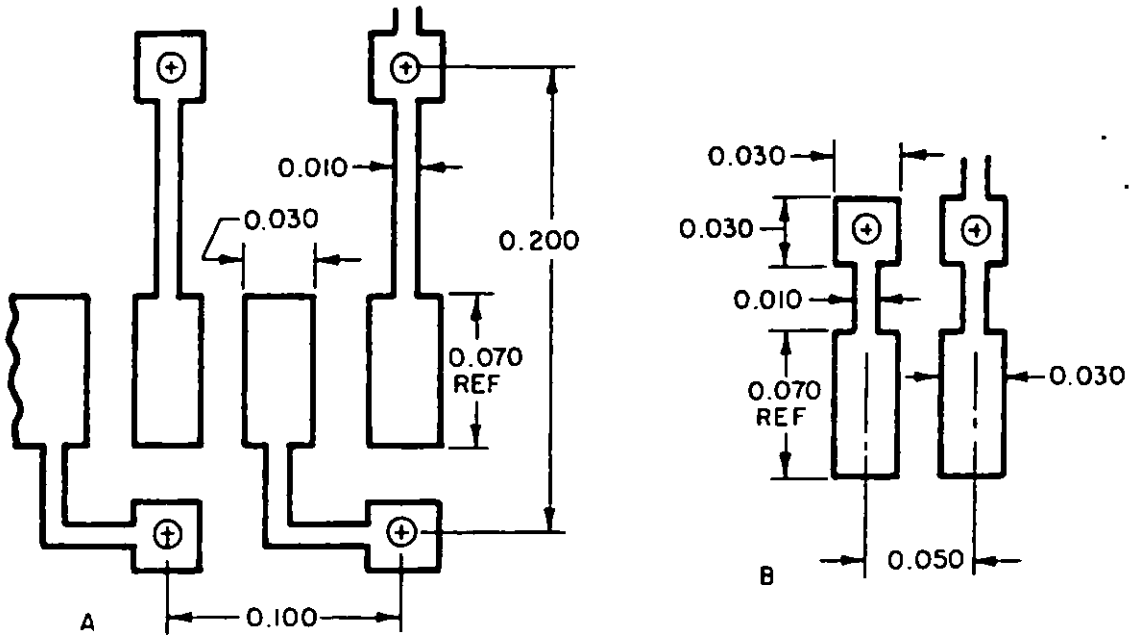


FIGURE 7. Modified fan-out patterns.

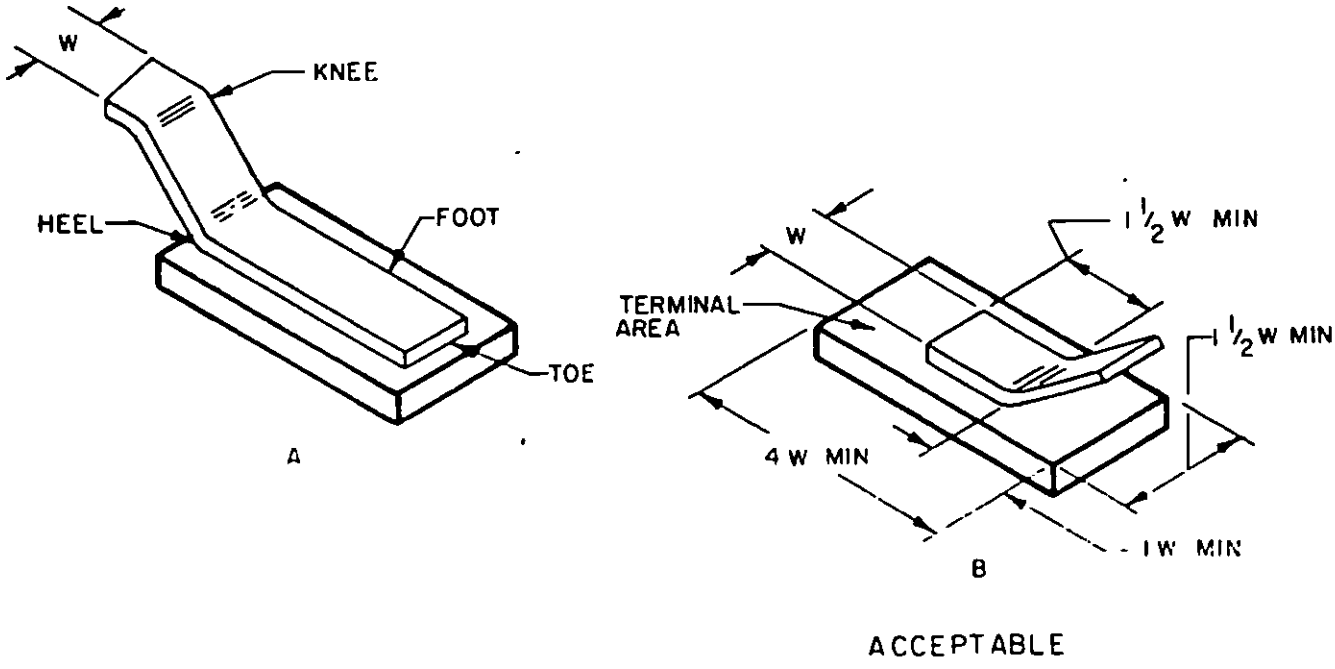


FIGURE 8. Heel mounting requirements.

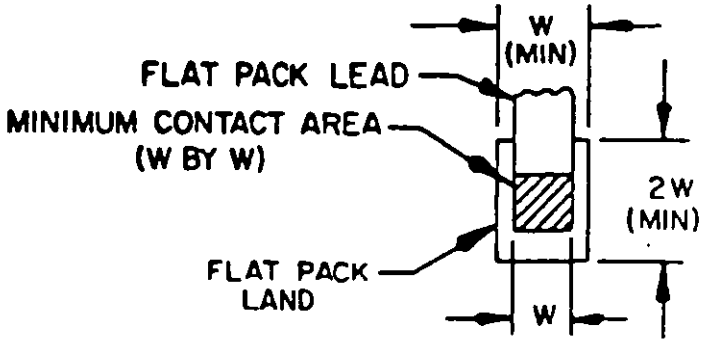


FIGURE 9. Typical flat pack land.

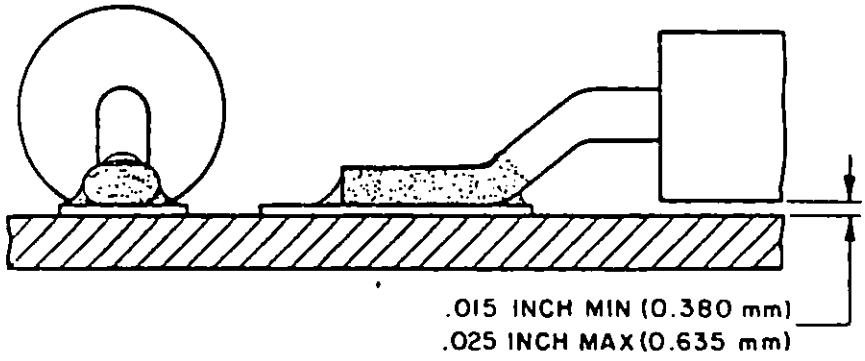


FIGURE 10. Coined or flattened lead.

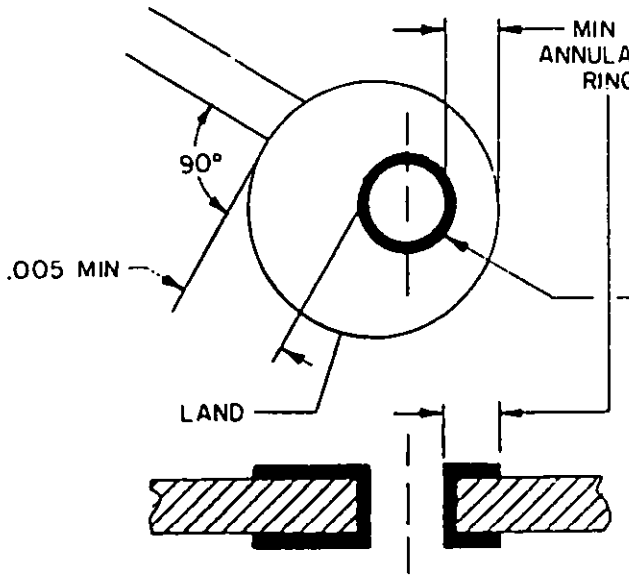


FIGURE 11. Minimum annular ring. (External) Type 2 or 3 boards.

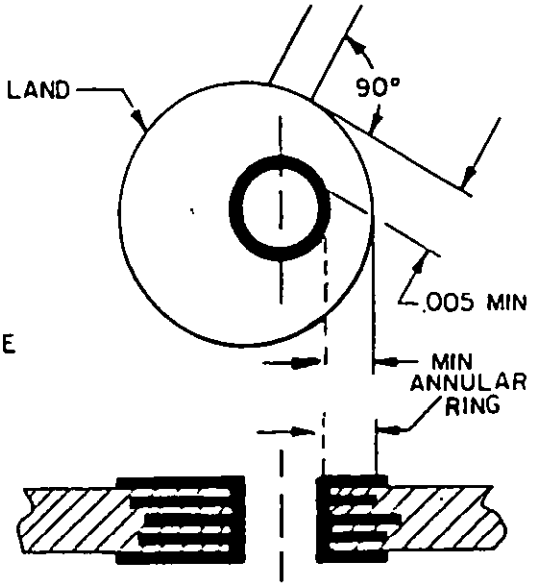
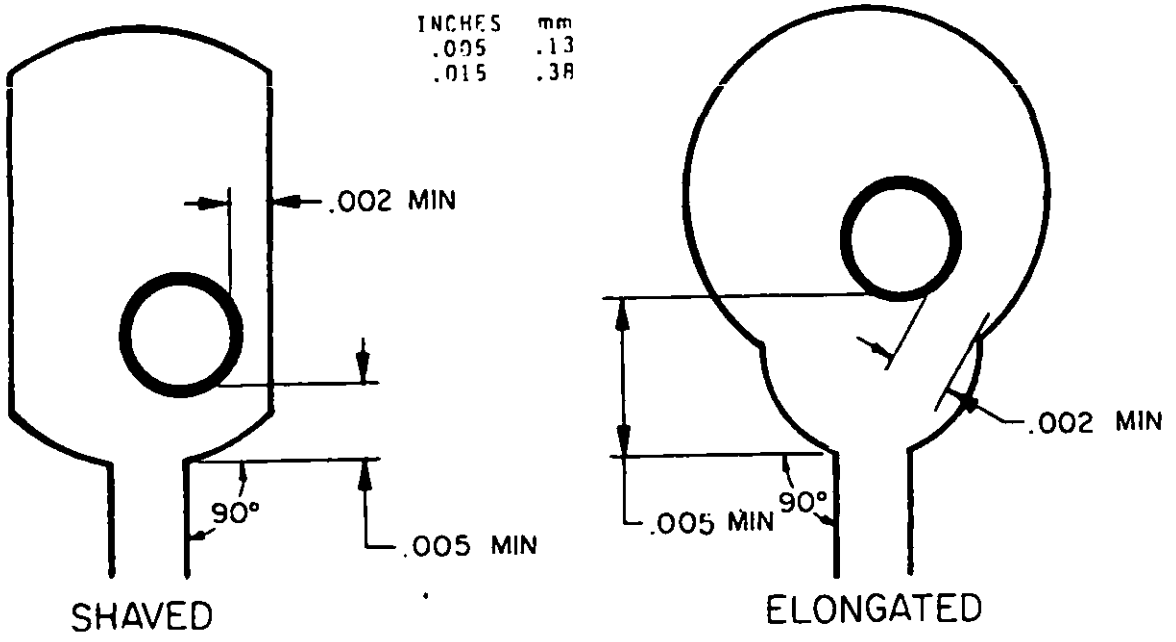
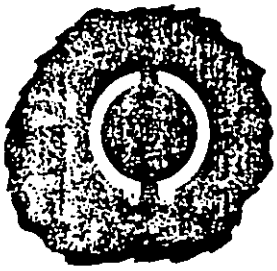


FIGURE 12. Minimum annular ring. (Internal) Type 3 boards.

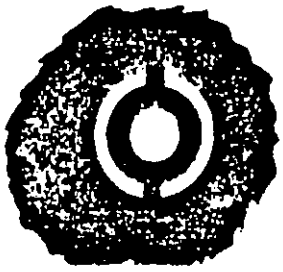


NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Radii are permissible at the junction of lands and conductors.

FIGURE 13. Examples of minimum annular ring dimensions. (External)

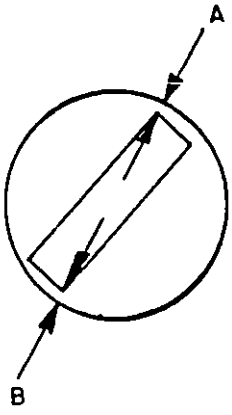


TERMINAL AREA BEFORE DRILLING



TERMINAL AREA AFTER DRILLING

FIGURE 14. Ground plane lands (typical).



	Plated-through hole	Unsupported hole
A + B =	.028 Inch (0.71 mm) MAX	.020 Inch (0.51 mm) MAX
	.006 Inch (0.15 mm) MIN	.006 Inch (0.15 mm) MIN

FIGURE 15. Hole diameter for flat lead.

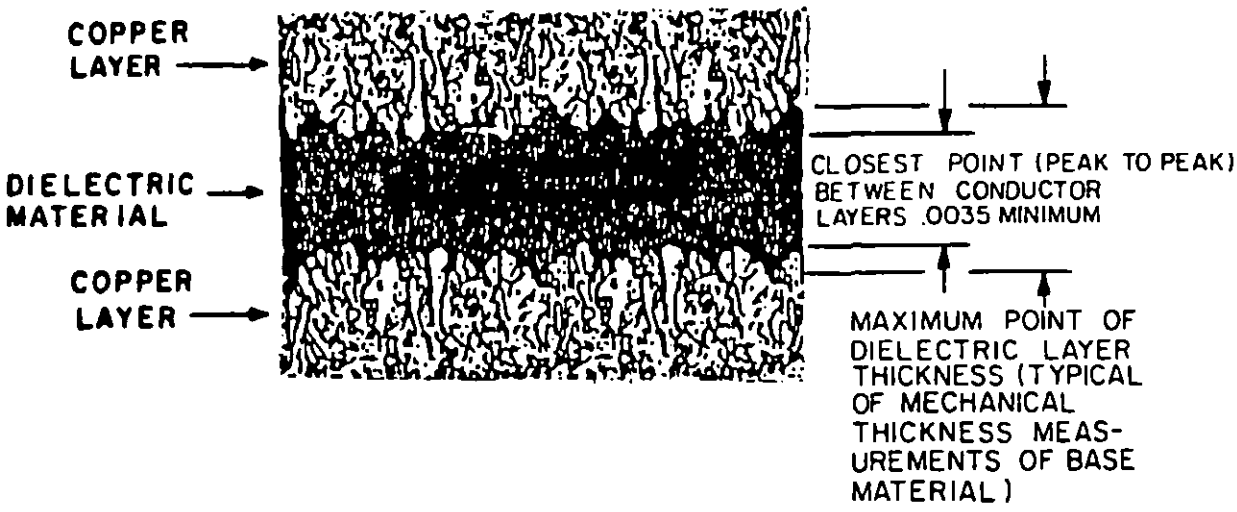
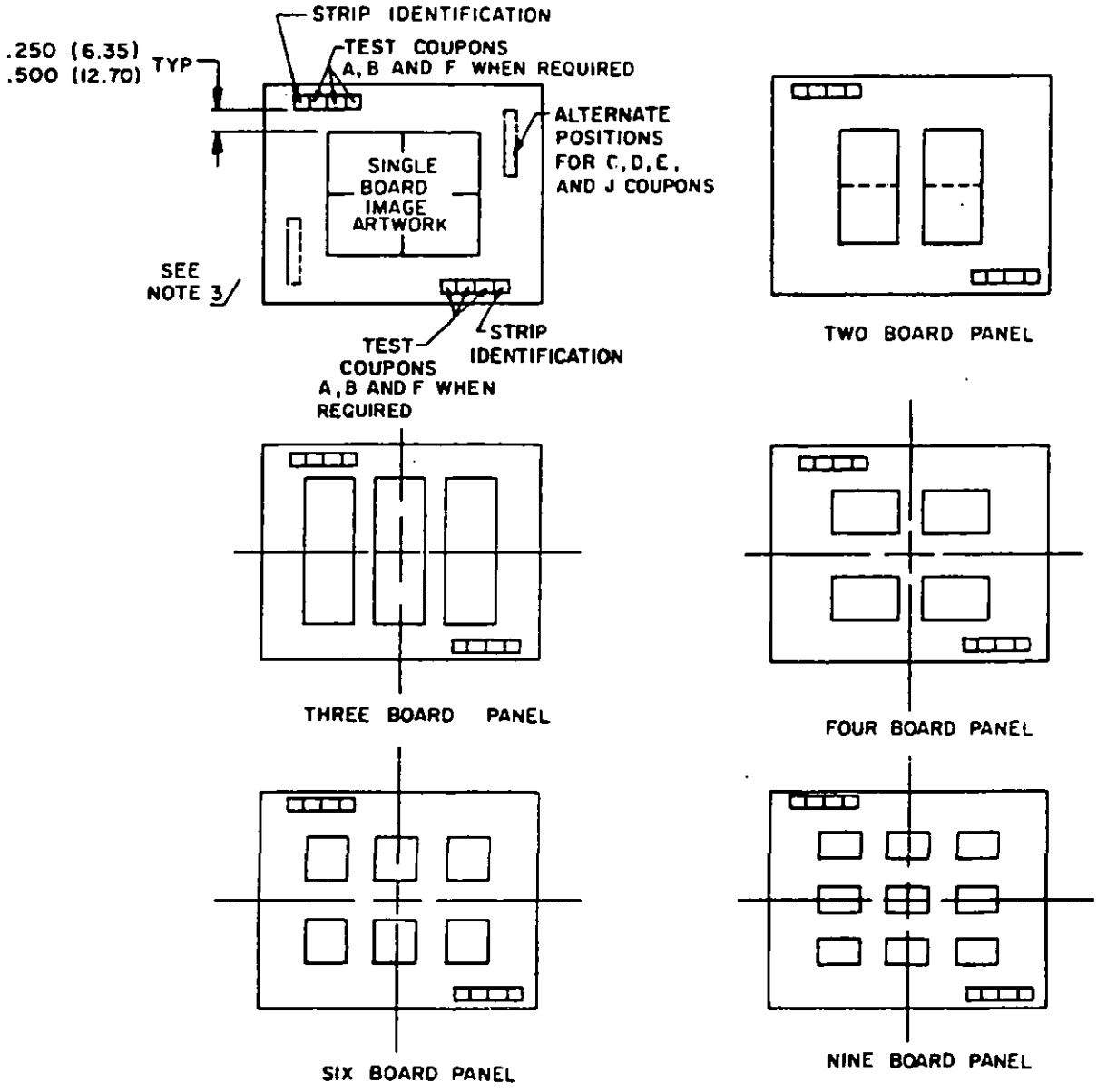


FIGURE 16. Dielectric layer thickness measurement.



NOTES:
1. Dimensions are in inches.
2. Metric equivalents are in parentheses.
3. Other coupons as required for use by fabricator to position on panel. Location on artwork is optional and location on panel is optional.

FIGURE 17. Location of test circuitry based on number of boards fabricated per panel.

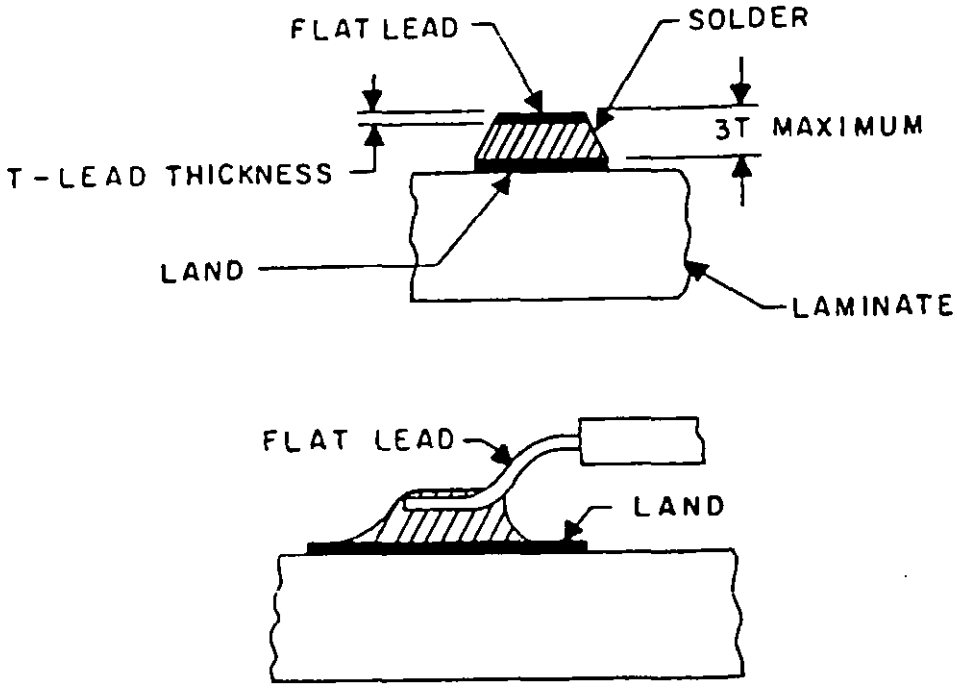
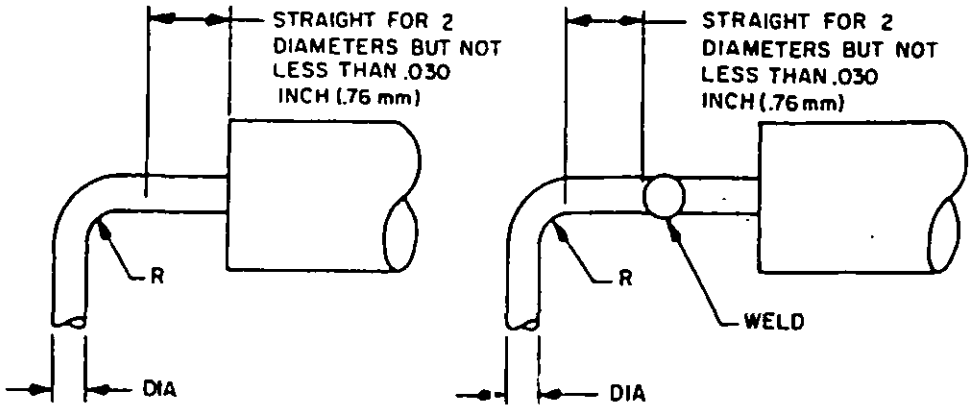


FIGURE 18. Flat lead termination.



A. STANDARD BEND

B. WELDED BEND

NOTE: Measurement shall be made from the end of the part. (The end of the part is defined to include any coating meniscus, solder seal, solder or weld bead, or any other extension.) (For figure 19B).

Lead diameter in inch	Minimum radius (R) inch
Up to .027 (0.69 mm)	1 diameter
From .028 (0.71 mm) to .047 (1.19 mm)	1.5 diameters
.048 (1.22 mm) and larger	2 diameters

FIGURE 19. Lead bend.

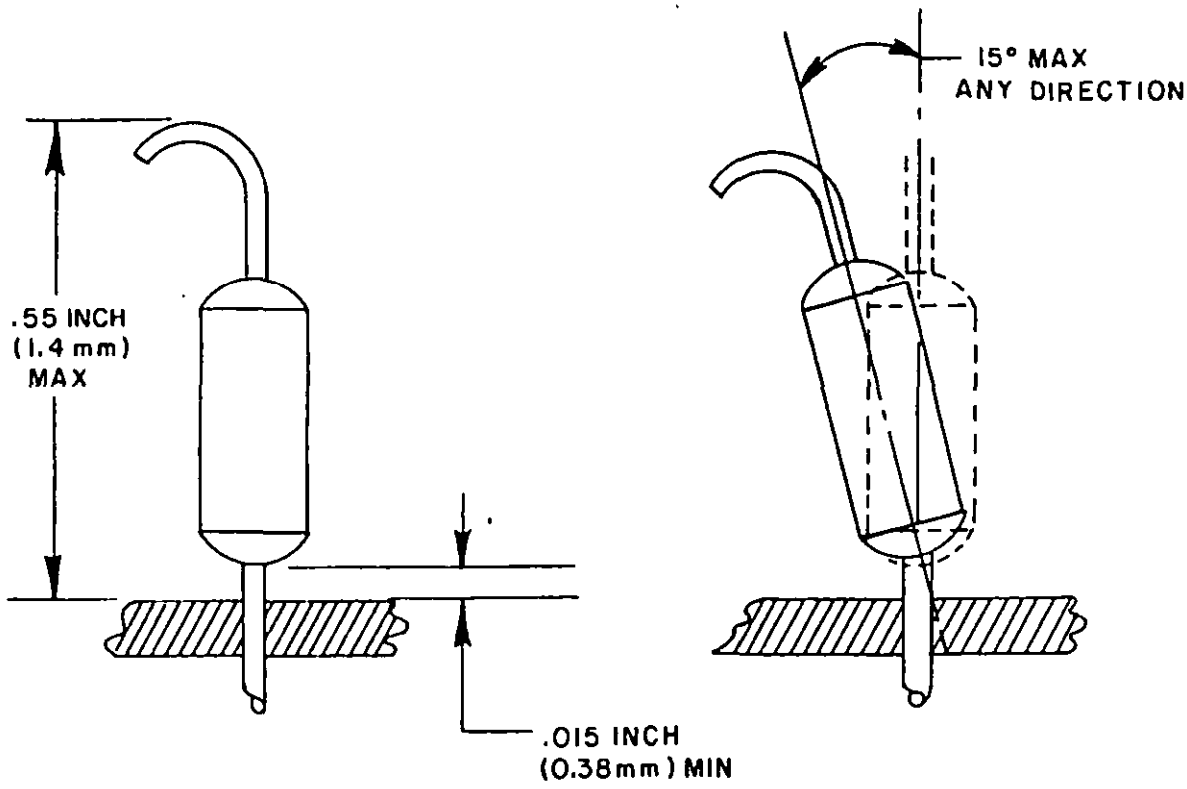


FIGURE 20. Perpendicular part mounting.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, EA, MI
Navy - OS, SH
Air Force - 11, 16, 85, 99
DLA - ES
NSA/S512

User activities:
Navy - AS, CG, MC
Air Force - 19

Agent:
DLA - ES

Preparing actitvity:
Navy - EC

(Project 5999-0146)