Input Source Impedance and Its Effects on DC-DC Converter Performance and Characteristics

Marco Panizza,
Manager, Europe Applications Engineering,
Vicor Corporation

Most power system designers employ the common rule to ensure the stability of DC-DC converters that the input source impedance should be small compared to the input impedance of the converter. Not all understand exactly why. It is also a common practice for most power system designers to use a large electrolytic capacitor across the input of the DC-DC converter.

This article is an analytical examination of the input impedance of a switch-mode DC-DC converter and the reasoning behind the common rule and the common practice.

Input Impedance of a Switch-mode DC/DC converter

A switch-mode DC-DC converter, regardless of its topology, presents negative incremental input impedance. This can be better understood by the following, qualitative reasoning.

A DC-DC converter works to maintain a constant output voltage, Vo, at a certain level of power, Po. To do this, it will absorb, from the input source, a power, Pi, given by:

$$P_I = \frac{P_O}{\eta} = V_I \cdot I_I$$

with η being the efficiency of the converter.

Let's assume that the input voltage decreases by a quantity $-\Delta V_I$. In order for the converter to sustain the output power, it will increase the input current by a quantity ΔI_I so that the input power stays constant at P_I. Assuming infinitesimal variation for V_I and I_I, it is possible to write:

$$\frac{dv_I}{di_I} = r_{I_d}$$

where r_{I_d} is the incremental input resistance. For a negative voltage variation, corresponding to a positive current variation; the incremental resistance will have a negative sign. The input resistance varies according to the input conditions because it depends from the input voltage at which the converter is working, as well as the output power that it is delivering.

For a 24 V input converter, with an input range of 18 – 36 V, working at 200 W load, the input current at 36 Vin will be:

$$I_I = \frac{P_I}{V_I} = \frac{P_O}{\eta \cdot V_I} = \frac{200}{0.83 \cdot 36} = 6.7A \Rightarrow r_I = \frac{V_I}{I_I} = \frac{36}{6.7} = -5.4\Omega$$

In the same conditions, if the voltage is reduced to 18V, the current will increase to 13.5 A and the resistance will be -1.33 Ω.

It is possible to repeat the same reasoning following a different approach [1]. Assuming that the converter is 100% efficient, input power and output power have the same value P, and it is possible to write:

$$r_I = \frac{dV_I}{dI_I} = \frac{d}{dI_I}\frac{P}{I_I} = -\frac{P}{{I_I}^2} = -\frac{V_I}{I_I} \qquad (1)$$

A switch-mode DC-DC converter can be seen as a DC transformer, having a transformation coefficient *n* defined as:

$$n = \frac{V_I}{V_O} = \frac{I_O}{I_I}$$

The coefficient *n* is dynamically adjusted, by the regulation loop, in order to keep the output voltage constant, regardless of the variations in load and input voltage. With this in mind, the equation (1) can be written as:

$$r_I = -\frac{nV_O}{\frac{I_O}{n}} = -n^2\frac{V_O}{I_O} = -n^2 R_L$$

where R_L is the load resistance. For a basic forward converter, the value *n* is:

$$n = \frac{1}{D}$$

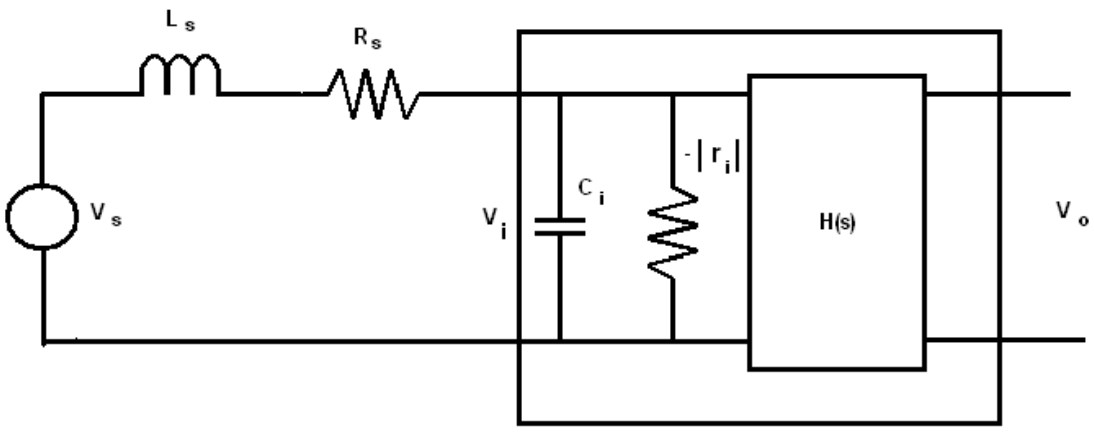
where *D* is the duty cycle of a pulse-width modulator (PWM) converter. In the case of a zero-current switching (ZCS) DC-DC converter, the control variable of the regulation loop is not the duty cycle, but the repetition frequency instead; therefore, as a first approximation:

$$r_I = -\frac{R_L}{f^2}$$

Influence of the Input Source Impedance on Stability

When a DC-DC converter works in a real application, it is connected to a power source having its own internal impedance that is not zero. Also, additional input impedance may be intentionally added, for example with an input EMI filter.

The complete block diagram hence can be drawn as this:



Here, the negative incremental input impedance is indicated as $-|r_i|$. Further, an additional internal capacitor C_i has also been added, as this is the typical case, at the input stage of a DC/DC converter.

Calling H(s) the transfer function of the DC/DC converter,

$$H(s) = \frac{V_o}{V_I}$$

the overall transfer function, including the input source impedance, will result:

$$\frac{V_O}{V_S} = H(s)\frac{Z_P}{Z_P + Z_S} \qquad (2)$$

This can also be written as:

$$\frac{V_O}{V_S} = H(s)\frac{1}{1+\frac{Z_S}{Z_P}}$$

As a general design rule, from the formula above it results that, if $Z_S << Z_P$ then the transfer function H(s) is not affected by the input source impedance. From this observation derives the general practical rule of keeping the source impedance at least ten times smaller than the internal DC/DC converter input impedance. It is possible, however, to study more accurately the source impedance effects, by using a detailed model, as shown above.

In this case, it is possible to write:

$$Z_P = -|r_i| // x_C = \frac{-|r_i|\frac{1}{sC_i}}{-|r_i|+\frac{1}{sC_i}} = \frac{-|r_i|}{1-s|r_i|C_i}$$

and

$$Z_S = R_S + sL_S$$

Replacing in (2) will result:

$$\frac{V_O}{V_S} = H(s)\frac{\frac{-|r_i|}{1-s|r_i|C_i}}{R_S + sL_S - \frac{|r_i|}{1-s|r_i|C_i}} = \frac{|r_i|}{s^2 L_S C_i |r_i| + s(|r_i|C_i R_S - L_S) + |r_i| - R_S} H(s) \qquad (3)$$

To verify the effect of the source impedance on the converter stability, it is possible to analyze the roots of the characteristic equation of (3), and by the Nyquist criteria, impose (ensure?) that these will fall in the left half plane of complex domain.

The characteristic equation can be written as:

$$s^2 L_S C_i + s\left(C_i R_S - \frac{L_S}{|r_i|}\right) + \left(1 - \frac{R_S}{|r_i|}\right) = 0$$

Being a quadratic equation, the roots are:

$$s_{1,2} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

where

$$a = L_S C_i$$

$$b = \left(C_i R_S - \frac{L_S}{|r_i|} \right)$$

$$c = 1 - \frac{R_S}{|r_i|}$$

With $a > 0$, for $s_{1,2}$ to have negative real part, it is necessary that $b > 0$ and $c > 0$; therefore:

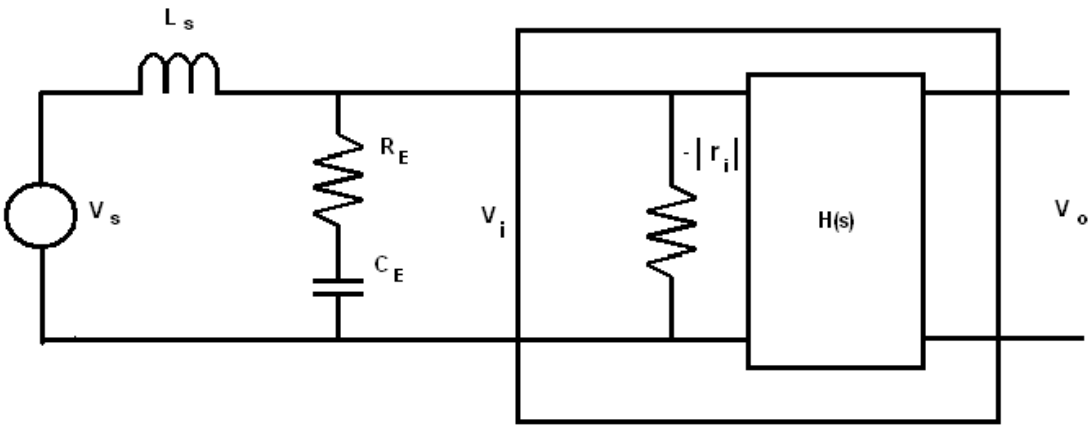
$$C_i R_S - \frac{L_S}{|r_i|} > 0 \Rightarrow R_S > \frac{L_S}{C_i |r_i|} \qquad (4)$$

and

$$1 - \frac{R_S}{|r_i|} > 0 \Rightarrow R_S < |r_i| \qquad (5)$$

Analyzing the results in (4) and (5), there is an important remark to be made. In fact, one obvious condition is that $R_S < |r_i|$ as discussed in the general case. However, according to (4), R_S cannot be arbitrarily small. In fact, if R_S is made too small, such as to violate (4), the system will show instability, because the RLC input network will be under-damped.

Another practical approach when designing input stages for a DC/DC converter is the common practice of adding a large capacitor in parallel. In this case the block diagram will result like this:



Compared to the previous schematic, the resistance R_S has been removed to simplify the analysis. This is, in general, an advantage, because a resistive element in series with the input lead causes power dissipation and penalizes the overall efficiency. The resistance R_E is the equivalent series resistance (ESR) of the capacitor C_E.

The internal capacitor C_i has also been removed. As an approximation, it can be considered as being part of C_E. Although this is not completely correct from the model standpoint, it could be enough to show the overall effect on stability. This simplification avoids generating a third-order equation that is more difficult to study.

As before, the overall transfer function of the circuit is:

$$\frac{V_O}{V_S} = H(s)\frac{Z_P}{Z_P + Z_S}$$

where:

$$Z_p = \frac{1}{\frac{1}{-|r_i|} + \frac{1}{R_E + \frac{1}{sC_E}}} = \frac{|r_i|(1 + sR_E C_E)}{sC_E(|r_i| - R_E) - 1}$$

Replacing in the transfer function, it results:

$$\frac{V_O}{V_S}=\frac{\dfrac{|r_i|(1+sR_EC_E)}{sC_E(|r_i|-R_E)-1}}{sL_S+\dfrac{|r_i|(1+sR_EC_E)}{sC_E(|r_i|-R_E)-1}}H(s)=\frac{|r_i|(1+sR_EC_E)}{s^2L_SC_E(|r_i|-R_E)+s(C_ER_E|r_i|-L_S)+|r_i|}H(s)$$

Dividing by $|r_i|$, it is possible to rewrite as:

$$\frac{V_O}{V_S}=\frac{1+sR_EC_E}{s^2\dfrac{L_SC_E(|r_i|-R_E)}{|r_i|}+s\left(C_ER_E-\dfrac{L_S}{|r_i|}\right)+1}H(s)$$

The stability can be studied by solving the roots of the left complex plane characteristic equation:

$$s^2\frac{L_SC_E(|r_i|-R_E)}{|r_i|}+s\left(C_ER_E-\frac{L_S}{|r_i|}\right)+1=0$$

This is a quadratic equation with solutions:

$$s_1,s_2=\frac{-b\pm\sqrt{b^2-4a}}{2a}$$

where

$$a=\frac{L_SC_E(|r_i|-R_S)}{|r_i|}\qquad\qquad b=\left(C_ER_E-\frac{L_S}{|r_i|}\right)$$

For the roots to be negative, both a and b must be positive, therefore it results:

$$\frac{L_SC_E(|r_i|-R_E)}{|r_i|}>0\Rightarrow|r_i|-R_E>0\quad\boxed{|r_i|>R_E}\qquad(6)$$

and,

$$C_ER_E-\frac{L_S}{|r_i|}>0\Rightarrow\boxed{\frac{L_S}{C_ER_E}<|r_i|}\qquad(7)$$

Equation (6) states that R_E should be smaller than $|r_i|$.

However, from (7) it is clear that if R_E is made too small, for example, by using high-quality input capacitors for C_E, the system could be under-damped and start to oscillate. For this reason, ceramic and film input capacitors are not recommended to restore the voltage source because the construction of these parts results in lower ESRs than electrolytic ones.

From (7) it is also possible to see that, the bigger the input inductance, the larger the required input capacitance, to compensate its effects. Also, for low-voltage systems such as a 12 V DC-DC converter that have lower input differential resistance r_i, larger input capacitance is needed to ensure stable operation.

Once the value of the input inductor L_S and input incremental resistance r_i are known, it is possible to replace the numbers in (6) and (7) to find the optimal combination for C_E with the proper ESR.

References:

[1] R.D. Middlebrook – "Input filter considerations, in design and application of switching regulators" 1976 IEEE